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# Houston13

CPU : Arrandale SV BGA  
Chip Set : Intel HM55(Ibex Peak)  
GFX : N11M -GE2-S(small pkg)  
Remarks : Calpella Platform

Model Name : Houston 13  
PBA Name : MAIN  
PCB Code : BA41-xxxxxA  
Dev. Step : PVR  
Revision : 1.0  
T.R. Date : 2010.4.2

Design	CHECK	APPROVAL

■ Owner : SEC Mobile R & D      Signature : X

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sheet03 : Cover  
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sheet53 : Power - Switched Power 2  
sheet54 : ICT FREE

DRAW	HONGJUN ZHAO,	DATE	10/10/2008	TITLE	Houston13 SV BGA	SAMSUNG ELECTRONICS
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		MAIN	
APPROVAL	BC LEE,	REV	1.0		COVER	
MODULE CODE		LAST EDIT	January, 16, 2010 4:17:48 PM	PAGE	1	OF 53

The diagram illustrates the system architecture, centered around the MCP (Arrandale SV BGA 133MHz) and PCH (IBEX PEAK). The MCP is connected to various power and logic components, including a CPU DC/DC converter, P1.1V\_VTT, P5.0V\_ALW, P3.3V\_AUX, GFX VR, P1.8V, Charging Circuit, and Smart Battery Module. It also connects to DDR 3 SODIMM 0 and 1, and a DDR 3 Power supply. The PCH is connected to a variety of peripheral components, including USB ports, Bluetooth, Camera, HD Audio, SATA HDD, SATA ODD, SUB BD, SPI ROM, MICOM, Touch PAD, KBD, SD(SDHC), MMC, and a 3 in 1 (GL827S) card reader. The diagram also shows connections for a FAN, CPU Thermistor, Clocking, HDMI, LCD, CRT, and a High Definition Audio section with HP MIC-IN and speakers. A watermark 'Confidential' is visible across the diagram.

DRAW	HONGJUN ZHAO,	DATE	10/10/2008	Houston13 SV BGA MAIN BLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK	ROCKY ZHENG,	DES. STEP	ADV1		
APPROVAL	BC LEE,	REV	1.0		
MODULE CODE	LAST EDIT				
				January 16, 2010 4:17:48 PM	PAGE 2 OF 53

BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails	Active in
VDC P3.3V_MICOM P5.0V_ALW P5.0V_STB	Primary DC system power supply (7 to 21V) 3.3V always power rail (for Micom) 5.0V always power rail 5.0V always power rail
P5.0V_AUX P3.3V_AUX P1.5V_AUX	5.0V switched on power rail (off in S4-S5) 3.3V switched on power rail (off in S4-S5) 1.5V power rail for DDR (off in S4-S5)
P5.0V P3.3V P1.8V P1.5V P0.75V	5.0V switched power rail (off in S3-S5) 3.3V switched power rail (off in S3-S5) 1.8V switched power rail (off in S3-S5) 1.5V switched power rail (off in S3-S5) 0.9V power rail for DDR (off in S3-S5)
VCC_CORE EGFX_CORE P1.05V (VCCP) P1.1V_VTT	Core Voltage for CPU Core Voltage for GPU VCC for Clarkfield & IBEX Peak VTT for CLARDSFIELD & IBEX Peak

USB PORT Assign		PCI Express Assign	
PORT #	ASSIGNED TO	PORT #	ASSIGNED TO
0	SYSTEM PORT 0	1	Mini Card 1 (WLAN)
1	SYSTEM PORT 1	2	NC
2	Multi Memory Card Controller	3	NC
3	NC	4	PCI-E LAN
4	NC	5	NC
5	NC	6	NC
6	NC	7	NC (N/A WITH HM55)
7	NC	8	NC (N/A WITH HM55)
8	TSP LCD		
9	SYSTEM PORT 9		
10	Bluetooth		
11	Camera		
12	NC		
13	NC		

SATA PORT Assign	
PORT #	ASSIGNED TO
0	HDD
1	ODD
2	(N/A WITH HM55)
3	(N/A WITH HM55)
4	e-SATA
5	

Crystal / Oscillator			
TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	IBEX-PEAK	Real Time Clock
Crystal	10MHz	MICOM	MEC1308-NU
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	88E8040-A0
Crystal	25MHz	IBEX PEAK	

LCD Pannel Detect (TBD)		
Devices	Resolution	PANNEL_DETECT_0

I <sup>2</sup> C / SMB Address			
Devices	Address	Hex	Bus
IBEX PEAK	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M Shrink(Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
Thermal Sensor on board	1101 100x	98h	
Power thermal management TS	1101 011x	96h	

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# POWER DIAGRAM

Rev 0.1

KBC3\_SUSPWR

KBC3\_PWRON

KBC3\_VRON

AC Adapter

Battery DC

VDC

P1.05V

ARD  
IBEX PEAK

VCC\_CORE

ARD

P1.05V\_D

OPTIMUS

IGFX\_CORE

OPTIMUS / INT GFX

EGFX\_CORE

OPTIMUS / EXT GFX

P1.5V\_AUX

DDR3 MEMORY  
PCH

P1.5V

P0.75V

DDR3 MEMORY

USB CONN

P5.0V\_ALW

When USB Charge Enable

P5.0V\_AUX

P5.0V

HDD FAN  
CRT PEG  
MICOM HDMI

P3.3V\_AUX

PCH  
LAN

P3.3V

IBEX PEAK  
MICOM  
HD AUDIO  
THERMAL SENSOR  
MINI PCIE  
MMC  
LCD  
DDR3  
LEDs  
BT

P3.3V\_MICOM

SPI ROM  
MICOM

P2.5V\_LAN

LAN

P3.3V\_D

OPTIMUS

P5.0V\_STB

P1.8V

IBEX PEAK

P12.0V\_ALW

P1.8V\_D

OPTIMUS

Power On/Off Table by S-state

Rail	S0	S3	S4	S5
State				
+V*(LWS) +V*LAN	ON	ON	ON	ON
+1.8V_AUX +0.9V	ON	ON	—	—
+V*AUX	ON	ON	—	—
+V	ON	—	—	—
+V* (CORE)	ON	—	—	—

S5-S4

S3

S0

DRAW	HONGJUN ZHAO,	DATE	10/10/2008	Houston13 SV BGA MAIN POWER DIAGRAM		SAMSUNG ELECTRONICS			
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1						
APPROVAL	BC LEE,	REV	1.0						
MODULE CODE		LAST EDIT		January, 16, 2010 4:24:56 PM		PAGE	4	OF	53

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**POWER RAILS ANALYSIS**

Rev. 0.6 (060920)

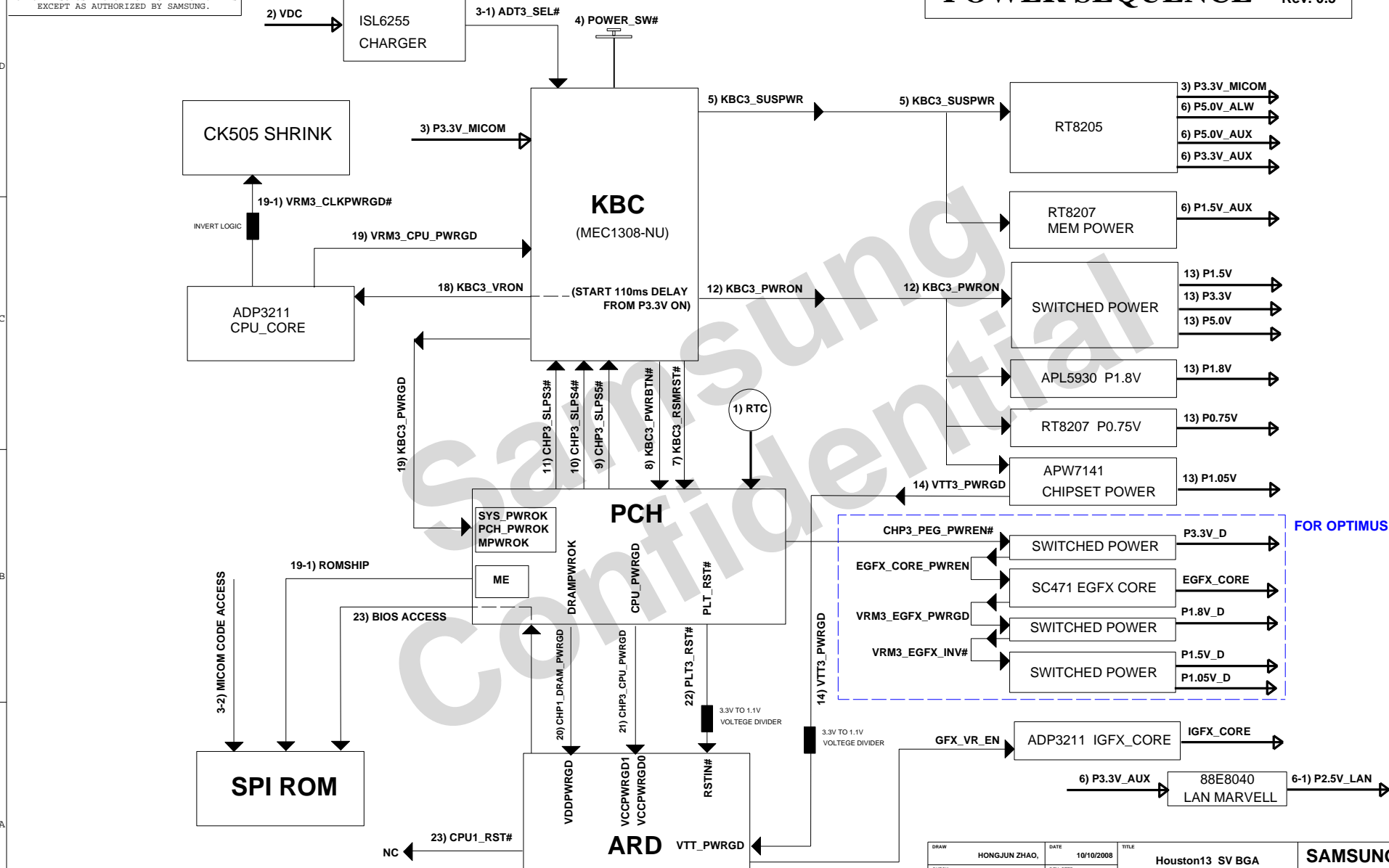
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Confidential

DRAW	HONGJUN ZHAO,	DATE	10/10/2008	TITLE	Houston13 SV BGA MAIN COVER	SAMSUNG ELECTRONICS PART NO. BA41-####A
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1			
APPROVAL	BC LEE,	REV	1.0			
MODULE CODE		LAST EDIT	January, 16, 2010 4:27:06 PM			
				PAGE	5	OF 53

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# POWER SEQUENCE

Rev. 0.5

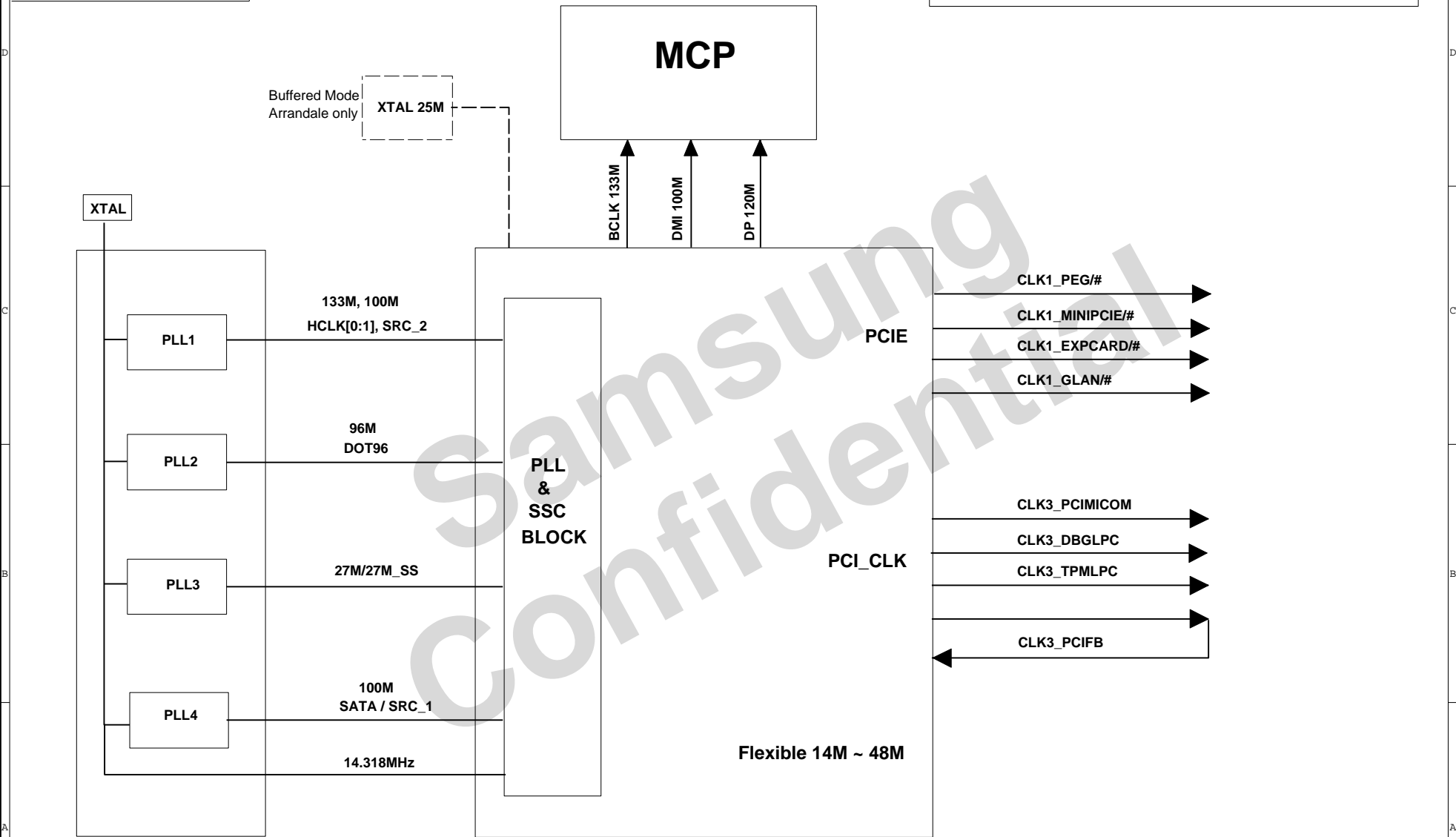


DRAW	HONGJUN ZHAO,	DATE	10/10/2008	TITLE	Houston13 SV BGA	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-####A
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		MAIN	
APPROVAL	BC LEE,	REV	1.0		POWER SEQUENCE	
MODULE CODE		LAST EDIT				
January, 16, 2010 4:28:57 PM						PAGE 6 OF 53

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# CLOCK DISTRIBUTION

Rev. 0.1



DRAW	HONGJUN ZHAO,	DATE	10/10/2008	TITLE	Houston13 SV BGA	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-####A
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		MAIN	
APPROVAL	BC LEE,	REV	1.0		CLOCK DIAGRAM	
MODULE CODE		LAST EDIT		January, 16, 2010 4:30:04 PM	PAGE 7 OF 53	

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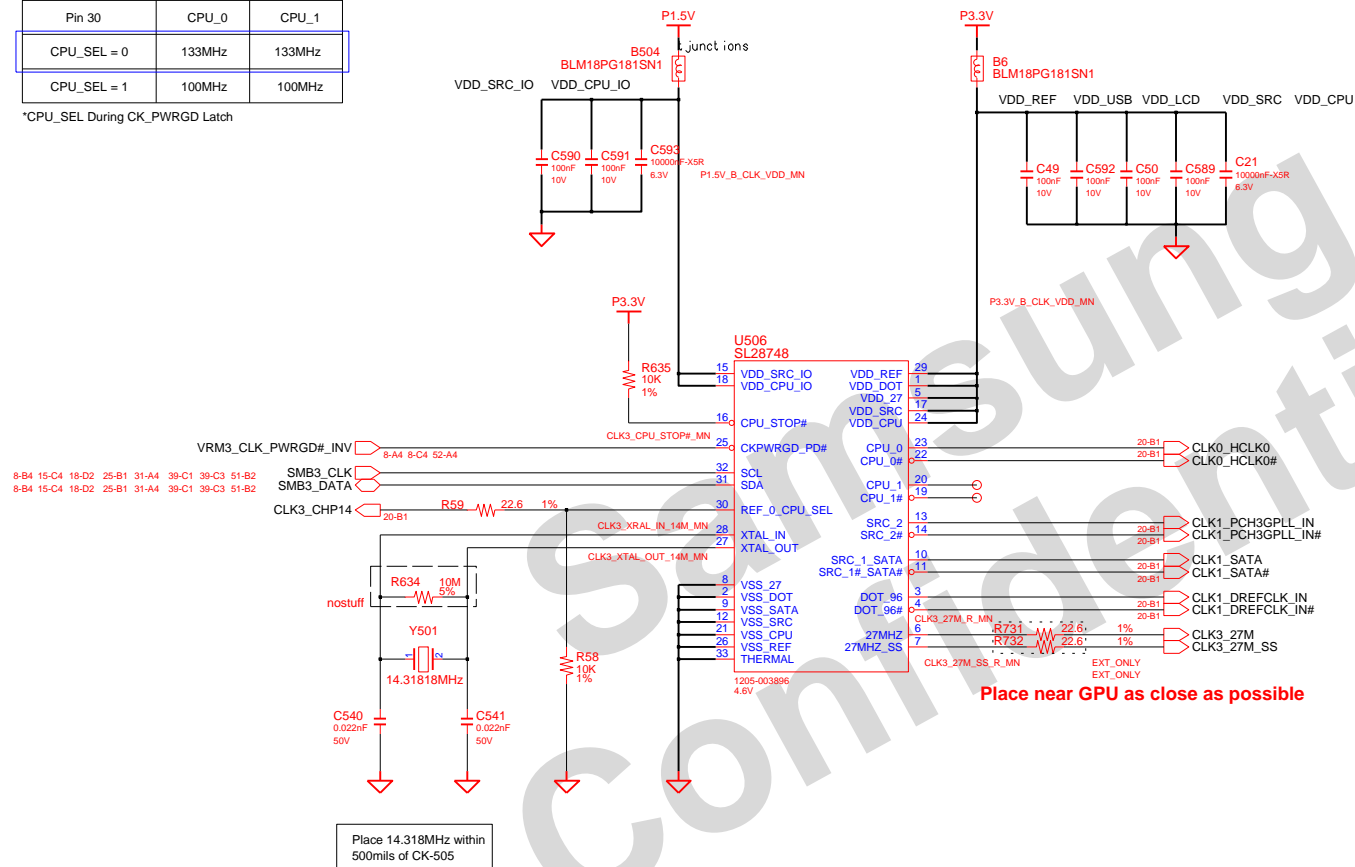
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## CK505M SHRINK VERSION

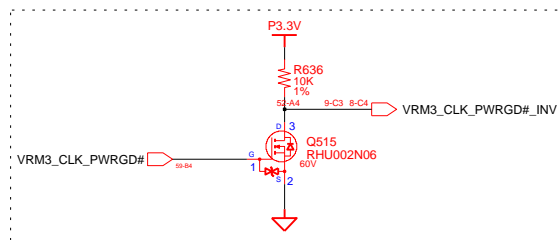
### CPU\_MODE SEL

Pin 30	CPU_0	CPU_1
CPU_SEL = 0	133MHz	133MHz
CPU_SEL = 1	100MHz	100MHz

\*CPU\_SEL During CK\_PWRGD Latch



Place near GPU as close as possible



DRAW	HONGJUN ZHAO,	DATE	10/10/2008	Houston13 SV BGA  CLOCK  CK505 SHRINK	SAMSUNG ELECTRONICS  PART NO. BA41-####A
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		
APPROVAL	BC LEE,	REV	1.0		
MODULE CODE		LAST EDIT			
				January, 16, 2010 4:31:36 PM	PAGE 8 OF 53



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## THERMAL SENSOR & FAN CONTROL

### MICOM RESET

ADDRESSSEL MODE	
0	0101 111xb
✓ HIGH Z	0111 101xb (7A)
1	0101 110xb

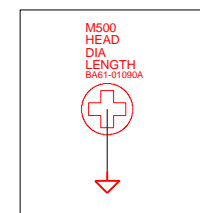
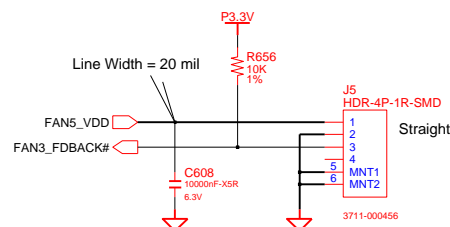
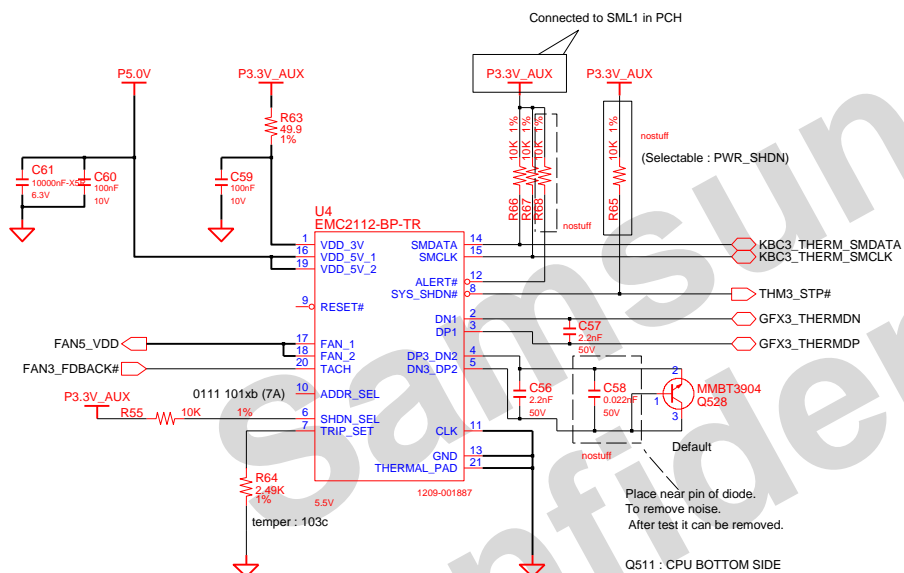
SHDNSEL MODE	
0	INTEL TR MODE
✓ HIGH Z	AMD CPU/DIODE MODE
1	EXT.DIODE 2 MODE

TRIP_SET Resistor Setting ( 60 ~ 122 C)	
60	0.0
✓ 95	1500
96	1580
97	1690
98	1820
99	1960
100	2050
101	2210
102	2370
103	2550
104	2740
105	2940
122	49900

$$V\_Trip = (T\_Trip - T\_Min) / 80$$

V\_TRIP : TRIP\_SET Voltage

T\_Min : Minimum Temperature



To Support Heatsink

DESIGN	HONGJUN ZHAO,	DATE	9/23/2008	TITLE	Houston13 SV BGA
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		THERMAL SENSOR
APPROVAL	BC LEE,	REV	REV 0.0		THERMAL SENSOR EMC2112
MODULE CODE	undefined	LAST EDIT	February, 22, 2010 9:47:19 AM	PAGE	9 OF 53


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PART NO. BA41-####A

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U15-1  
ARRANDALE

1.1K ohm / 3.01K ohm

DRAW	HONGJUN ZHAO,	DATE	9/23/2008	Houston13 SV BGA  CPU  SV BGA		
CHECK	ROCKY ZHEGN,	DEV. STEP	ADV1			
APPROVAL	BC LEE,	REV	REV 0.0			
MODULE CODE		LAST EDIT				

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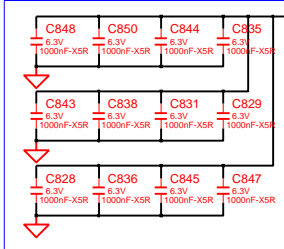
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APPROVAL	BC LEE,	REV	REV 0.0		PART NO.	BA14-####A	
MODULE CODE	undefined	LAST EDIT			February, 22, 2010 9:50:02 AM	PAGE	11 OF 53

ALL VTT DECAP IS SHARED

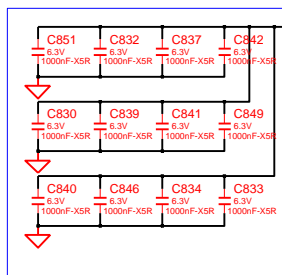
**\*\*VTT POWER SELECTION**

VTT_SEL	VOLTAGE	CPU
1	P1.05V	ARRANDALE
0	P1.1V	CLARKS FIELD

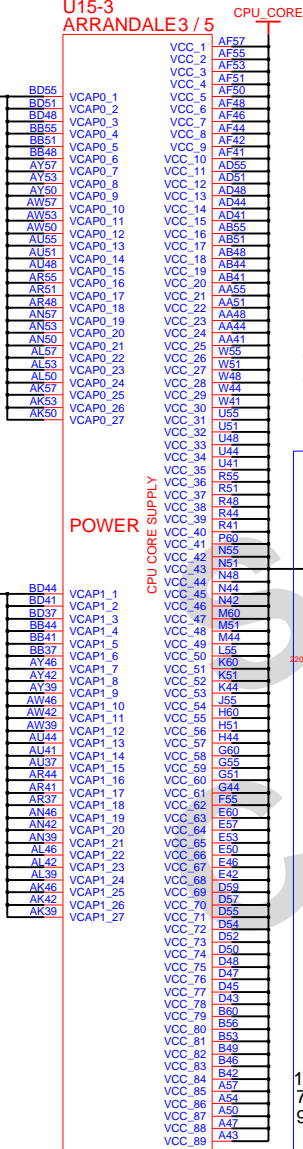
**Charger : PI**



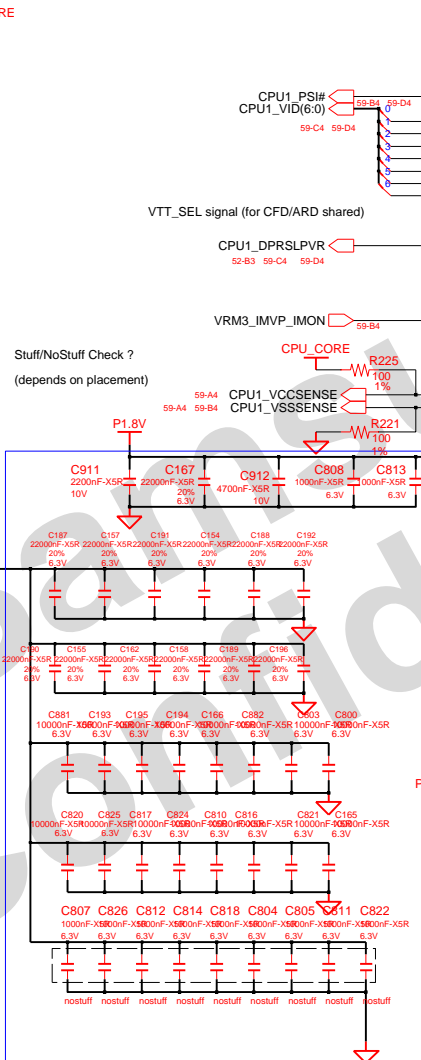
**Charger : PI**



**U15-3  
ARRANDALE3/5**

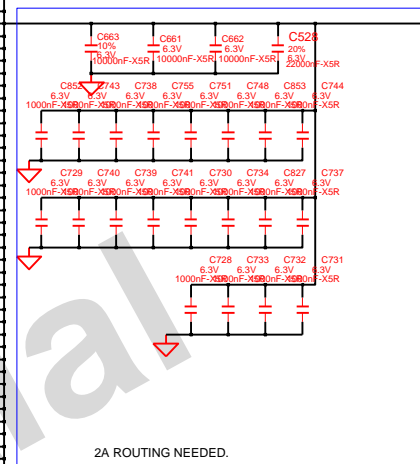
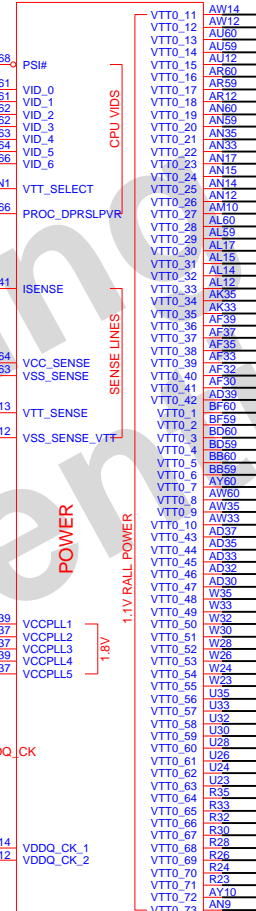


**POWER**

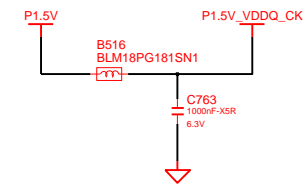


12 22uF Place inside cavity of the socket  
7 10uF Under cavity of the socket  
9 10uF Between inductor and socket on top layer

**Charger : PI**



**Charger : PI**



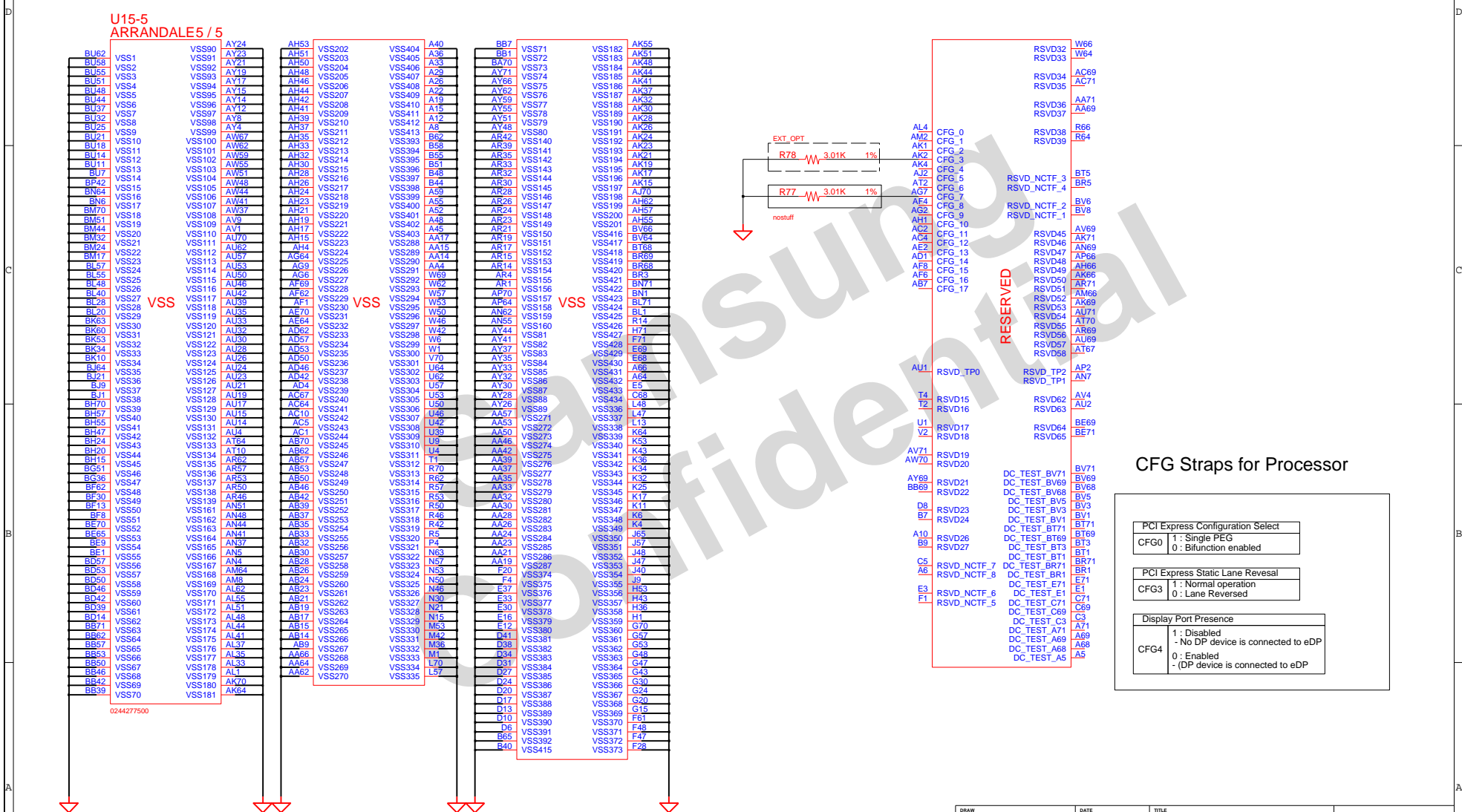
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APPROVAL	BC LEE,	REV	REV 0.0		SV BGA	
MODULE CODE	undefined	LAST EDIT	February, 22, 2010 9:50:54 AM	PAGE	12 OF 53	

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DESIGN	HONGJUN ZHAO,	DATE	8/19/2009	TITLE Houston13 SV BGA CPU SV BGA	SAMSUNG ELECTRONICS
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		
APPROVAL	BC LEE,	REV	REV 0.0		
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				PAGE	13 OF 53

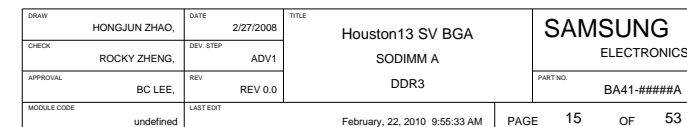
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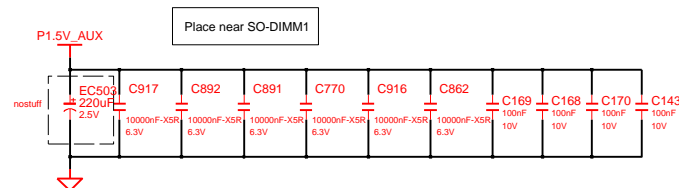
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CHECK	ROCKY ZHENG,	DEV. STEP	ADV1				
APPROVAL	BC LEE,	REV	REV 0.0		PART NO.	BA41-####A	
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P/N : 3709-001560 (Foxconn)

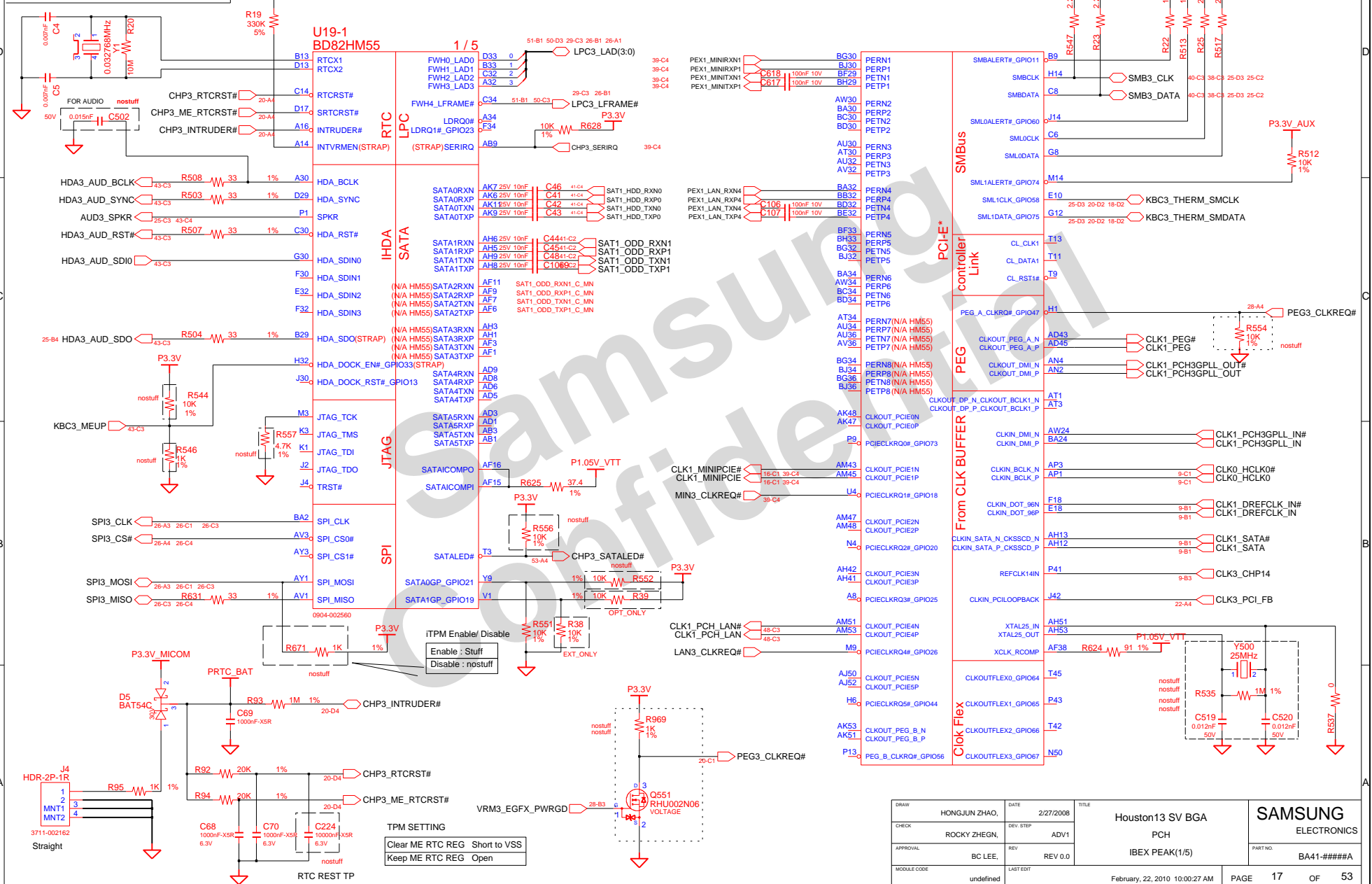


P/N : 3709-001559 (Foxconn)

D:/users/ecad42/Houston13/temp/0222/Houston13\_MAIN



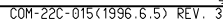
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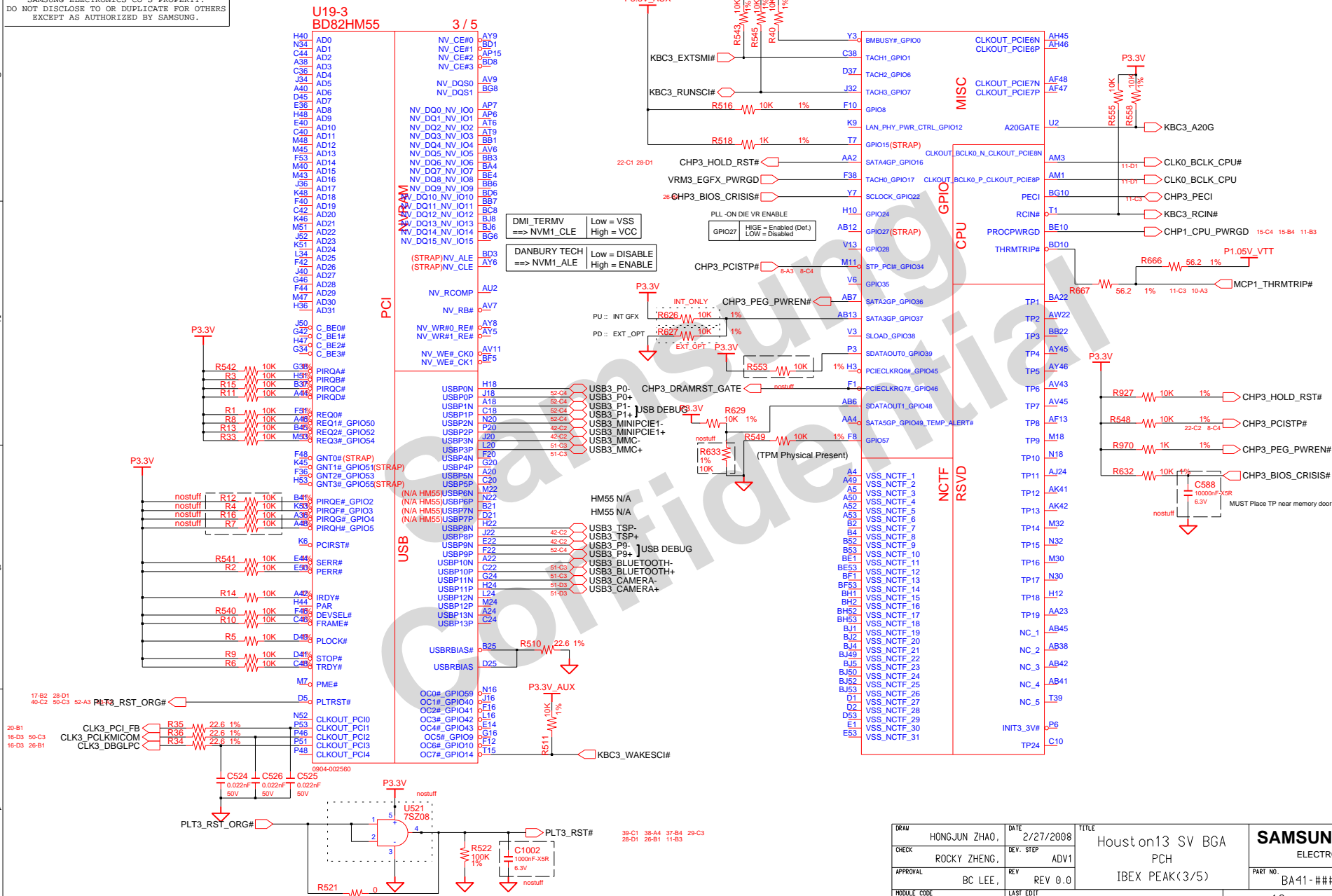


DRAW	HONGJUN ZHAO,	DATE	2/27/2008	TITLE	Houston13 SV BGA
CHECK	ROCKY ZHEGN,	DEV. STEP	ADV1		PCH
APPROVAL	BC LEE,	REV	REV 0.0		IBEX PEAK(1/5)
MODULE CODE	undefined	LAST EDIT	February, 22, 2010 10:00:27 AM	PAGE	17 OF 53

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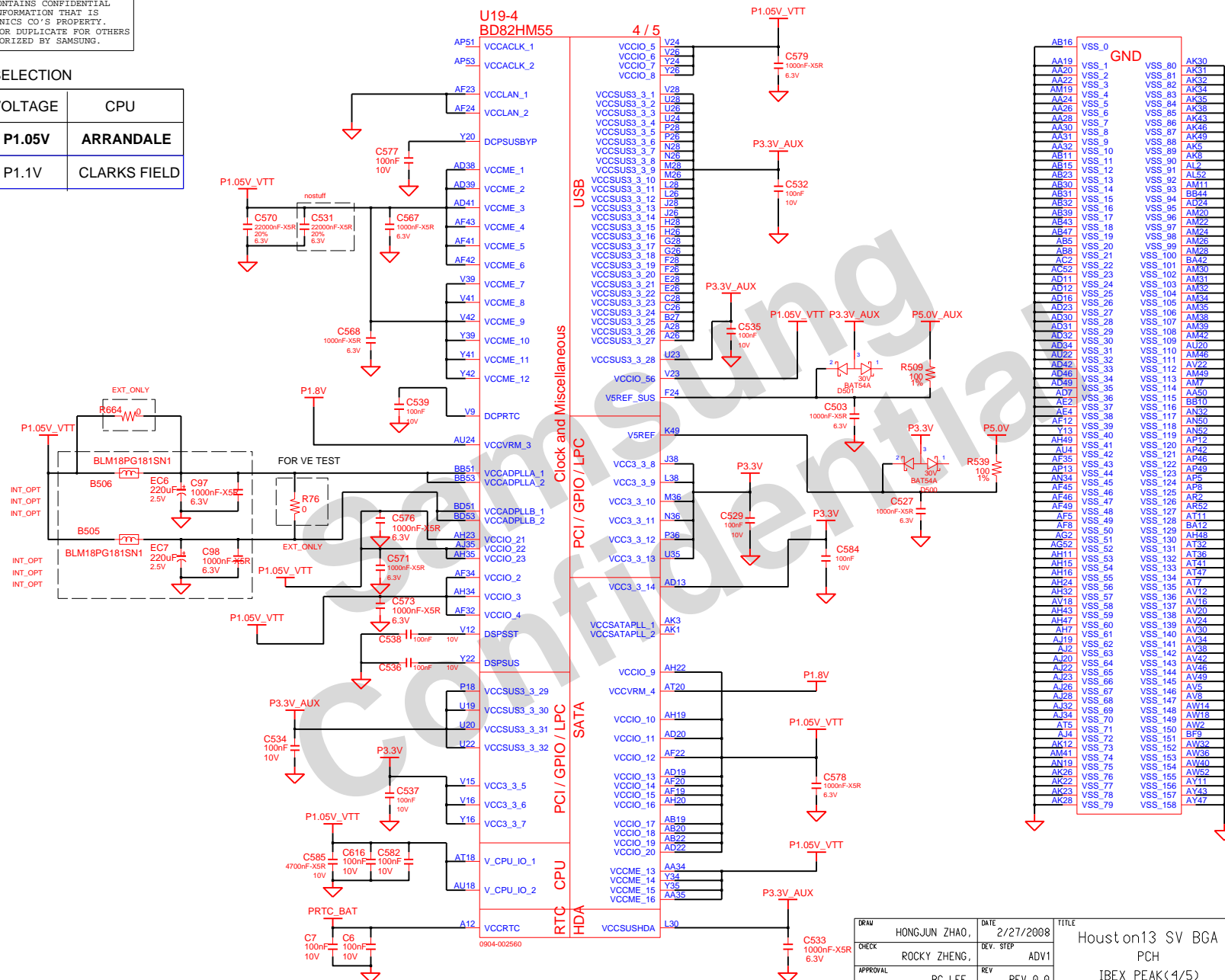
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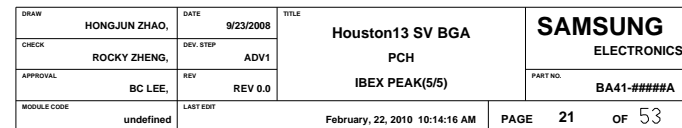
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VTT_SEL	VOLTAGE	CPU
1	P1.05V	ARRANDALE
0	P1.1V	CLARKS FIELD



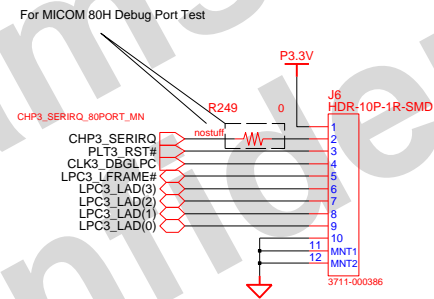
DRAM	HONGJUN ZHAO,	DATE	2/27/2008	TITLE Houston13 SV BGA PCH IBEX PEAK(4/5)	<b>SAMSUNG</b> ELECTRONICS
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		
APPROVAL	BC LEE,	REV	REV 0.0		
MODULE CODE	undefined	LAST EDIT	February, 22, 2010 10:13:38 AM		
				PAGE	20 OF 603

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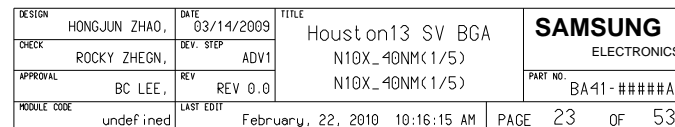
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# 80H PORT DEBUG



DESIGN	HONGJUN ZHAO,	DATE	11/10/2008	TITLE	Houston13 SV BGA	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-####A
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		DEBUG PORT	
APPROVAL	BC LEE,	REV	REV 0.0		80H DECODER	
MODULE CODE	undefined	LAST EDIT	February, 22, 2010 10:15:03 AM	PAGE	22	OF 53

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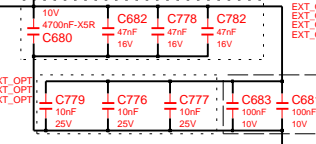
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U8-2  
N11M-GE2-S-B1 2 / 5

PEG1\_DQA(63:0)

0	D22	FBA D0	FBVDDQ_1
1	E22	FBA D1	FBVDDQ_2
2	E22	FBA D2	FBVDDQ_3
3	D24	FBA D3	FBVDDQ_4
4	D26	FBA D4	FBVDDQ_5
5	D27	FBA D5	FBVDDQ_6
6	C27	FBA D6	F13
7	B27	FBA D7	F13
8	A21	FBA D8	FBVDDQ_8
9	B21	FBA D9	FBVDDQ_9
10	C21	FBA D10	FBVDDQ_10
11	C19	FBA D11	FBVDDQ_11
12	C18	FBA D12	FBVDDQ_12
13	D18	FBA D13	FBVDDQ_13
14	B18	FBA D14	FBVDDQ_14
15	E21	FBA D15	FBVDDQ_15
16	F21	FBA D16	FBVDDQ_16
17	F21	FBA D17	FBVDDQ_17
18	D20	FBA D18	FBVDDQ_18
19	F20	FBA D19	FBVDDQ_19
20	D17	FBA D20	FBVDDQ_20
21	F18	FBA D21	FBVDDQ_21
22	D16	FBA D22	FBVDDQ_22
23	E16	FBA D23	FBVDDQ_23
24	A22	FBA D24	FBVDDQ_24
25	C24	FBA D25	FBVDDQ_25
26	D21	FBA D26	FBVDDQ_26
27	B22	FBA D27	
28	C22	FBA D28	
29	A25	FBA D29	
30	B25	FBA D30	
31	A26	FBA D31	
32	U24	FBA D32	
33	V23	FBA D33	
34	R24	FBA D34	
35	T23	FBA D35	
36	R23	FBA D36	
37	P24	FBA D37	
38	P22	FBA D38	
39	AC24	FBA D39	
40	AB23	FBA D40	
41	AB24	FBA D41	
42	AB24	FBA D42	
43	W24	FBA D43	
44	AA22	FBA D44	
45	W23	FBA D45	
46	W22	FBA D46	
47	V22	FBA D47	
48	AA25	FBA D48	
49	W27	FBA D49	
50	W26	FBA D50	
51	W25	FBA D51	
52	AB25	FBA D52	
53	AD26	FBA D53	
54	AD27	FBA D54	
55	V25	FBA D55	
56	R25	FBA D56	
57	V26	FBA D57	
58	V27	FBA D58	
59	R26	FBA D59	
60	T25	FBA D60	
61	N25	FBA D61	
62	N26	FBA D62	
63	N26	FBA D63	

P1.5V\_D



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CMD MODE A

PEG1\_DQMA(7:0)

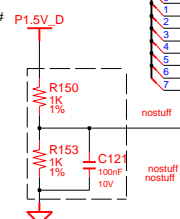
0	C26	FBA DQM0
1	B19	FBA DQM1
2	D23	FBA DQM2
3	D23	FBA DQM3
4	T24	FBA DQM4
5	AA23	FBA DQM5
6	AB27	FBA DQM6
7	T26	FBA DQM7

PEG1\_WDQSA(0:7)

FB\_DQS\_WP must be connected to DQSU#DQSL#  
@ gDDR3 component

PEG1\_RDQSA(0:7)

FB\_DQS\_RN must be connected to DQSU#DQSL#  
@ gDDR3 component



0904-002586

EXT\_OPT

FBA_CMD0	F26	PEG1_MAA(4)
FBA_CMD1	J24	PEG1_RASA#
FBA_CMD2	M23	PEG1_MAA(5)
FBA_CMD3	N27	PEG1_BAA1
FBA_CMD4	M27	PEG1_MAB(2)
FBA_CMD5	K26	PEG1_MAB(4)
FBA_CMD6	J25	PEG1_MAB(3)
FBA_CMD7	J27	
FBA_CMD8	G23	PEG1_CSA10#
FBA_CMD9	J23	PEG1_MAA(11)
FBA_CMD10	G26	PEG1_CASA#
FBA_CMD11	J25	PEG1_WEA#
FBA_CMD12	K27	PEG1_BAA0
FBA_CMD13	G25	PEG1_MAB(5)
FBA_CMD14	L24	PEG1_MAA(12)
FBA_CMD15	K23	PEG1_MAA(7)
FBA_CMD16	K24	PEG1_MAA(10)
FBA_CMD17	G22	
FBA_CMD18	H24	PEG1_MAA(9)
FBA_CMD19	H24	PEG1_MAA(6)
FBA_CMD20	H22	PEG1_MAA(8)
FBA_CMD21	F27	PEG1_MAA(2)
FBA_CMD22	M26	PEG1_MAA(8)
FBA_CMD23	J26	PEG1_MAA(3)
FBA_CMD24	G24	PEG1_MAA(1)
FBA_CMD25	G27	PEG1_MAA(13)
FBA_CMD26	M24	PEG1_BAA2
FBA_CMD27	K22	
FBA_CMD28	J22	
FBA_CMD29	L22	PEG1_CSA00#
FBA_CMD30		
FBA_CLK0	F24	PEG1_CLKA0
FBA_CLK0_N	F23	PEG1_CLKA0#
FBA_CLK1	N24	PEG1_CLKA1
FBA_CLK1_N	N23	PEG1_CLKA1#
FBA_DEBUG	M22	

P1.5V\_D

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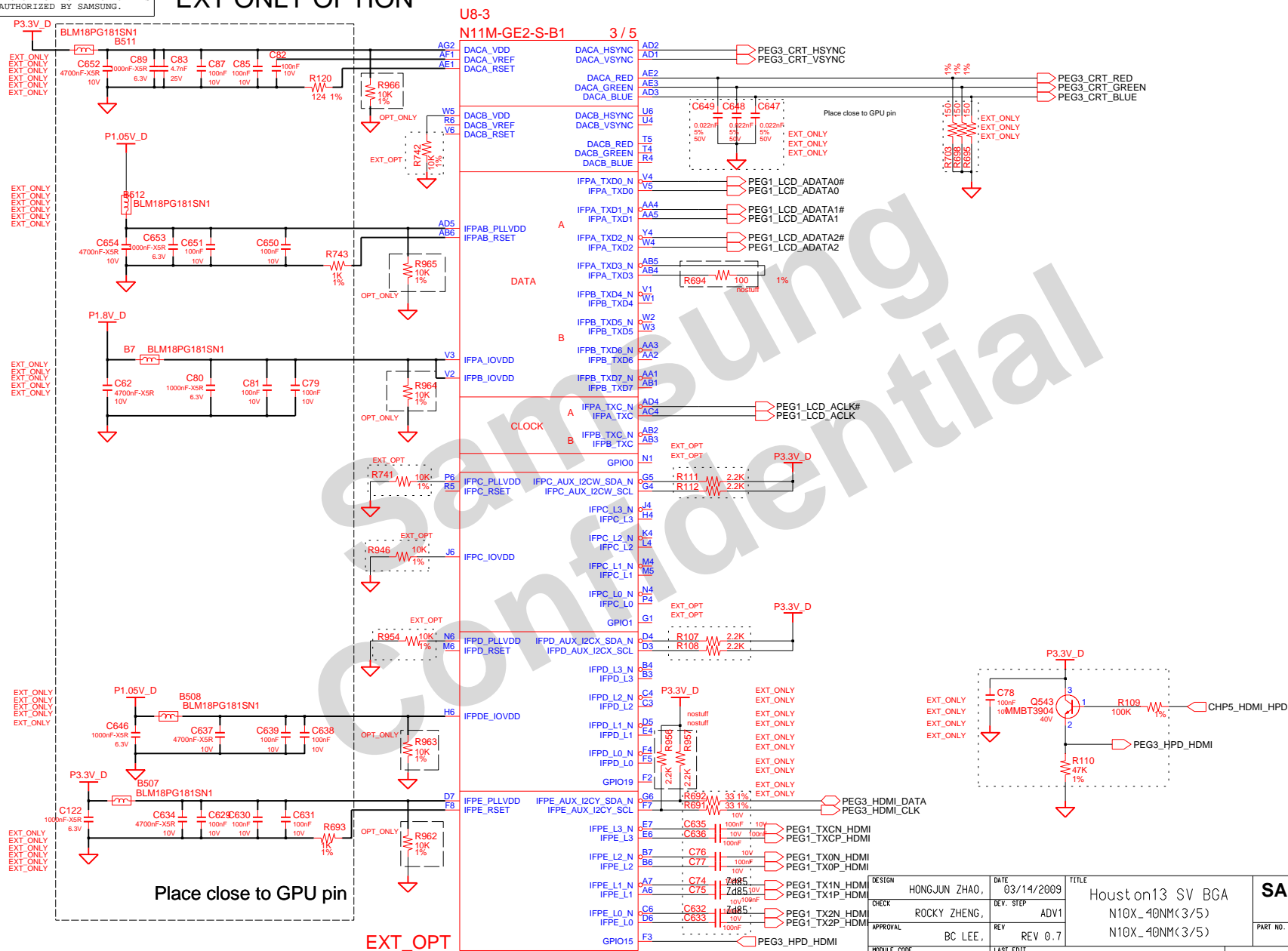
EXT\_OPT

EXT\_OPT

DESIGN	HONGJUN ZHAO,	DATE	03/14/2009	TITLE	Houston13 SV BGA	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-####A
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		N10X_40NM(2/5)	
APPROVAL	BC LEE,	REV	REV 0.0		N10X_40NM(2/5)	
MODULE CODE	undefined	LAST EDIT	February, 22, 2010 11:41:16 AM	PAGE	24 OF 53	



## EXT ONLY OPTION



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Pin	Description	Activate
GPIO(0)	General Purpose	NC
GPIO(1)	HPD-C	NC
GPIO(2)	LC0D_BL_PWM	High
GPIO(3)	LC0D_VDD	High
GPIO(4)	LC0D_BL_EN	High
GPIO(5)	GPU VID0	00 0.8V 10 0.95V
GPIO(6)	GPU VID1	01 0.85V 11 1.03V
GPIO(7)	GPU VID2	NC
GPIO(8)	oVERT	LOW
GPIO(9)	ALERT	NC
GPIO(10)	MEM_VREF	NC
GPIO(11)	SLI_SYNC	NC
GPIO(12)	PWR_LEVEL	NC
GPIO(13)	MEM_VID	NC
GPIO(14)	PWR_CTRL1	NC
GPIO(15)	HPD-E	High
GPIO(16)	FAN_PWM	NC
GPIO(17)	Reserved	NC
GPIO(18)	Reserved	NC
GPIO(19)	HPD-D	NC

Strap option	Bit 3	Bit 2	Bit 1	Bit 0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	<b>DEVID[4]</b>	VENID	CLK_CFG	PLL_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	<b>DEVID[3]</b>	<b>DEVID[2]</b>	<b>DEVID[1]</b>	<b>DEVID[0]</b>
STRAP1	PADCFG[3]	PADCFG[2]	PADCFG[1]	PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
Resistor value	PU to VDD	PD to GND	XCLK417 = 0.27MHz	
5K ohm	1000	0000	RAM CFG (SEC)	
10 Kohm	1001	0001	0011 gpDR3 1Gb	
15K ohm	1010	0010	USER[3:0]=1111 for EDID	
20K ohm	1011	0011	PADCFG[3:0]=0110 for N	
25K ohm	1100	0100		
30K ohm	1101	0101		
35K ohm	1110	0110		
45K ohm	1111	0111		

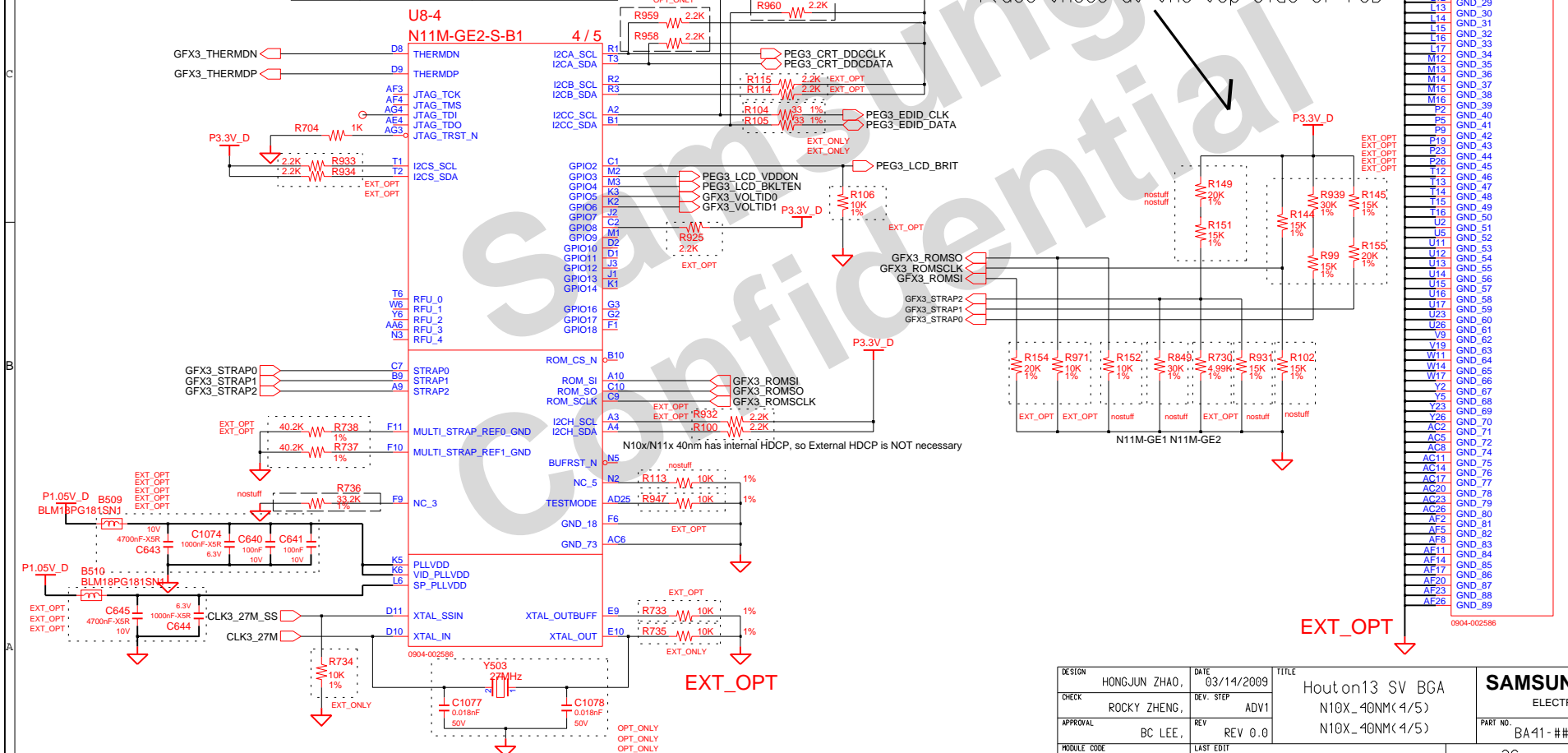
	Bit3	Bit2	Bit1	Bit0	
ROMSO	0	0	0	0	27M
SCLK	1	0	1	0	N11M-GE GFX TPYE
	0	0	1	0	N11M-LP1
SI	0	0	1	1	gDDR3 1Gb
Strap2	0	0	0	0	N11M-GE2
Strap2	0	1	0	1	N11M-GE1 DEVICE1
Strap1	1	1	1	0	PEG PCIE swing level
Strap0	1	1	1	1	EDID_EN

N11M-GE2-S-B1

5 / 5

N11M-GE2: 0x0A70

Place these at the top side of PCB



DESIGN	HONGJUN ZHAO,	DATE	03/14/2009	Houton13 SV BGA N10X_40NM(4/5) N10X_40NM(4/5)	<b>SAMSUNG</b> ELECTRONICS
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		
APPROVAL	BC LEE,	REV	REV 0.0		
MODULE CODE	undefined	LAST EDIT	February, 22, 2010 11:44:01 AM		
				PAGE	26 OF 53

## A-Channel #0

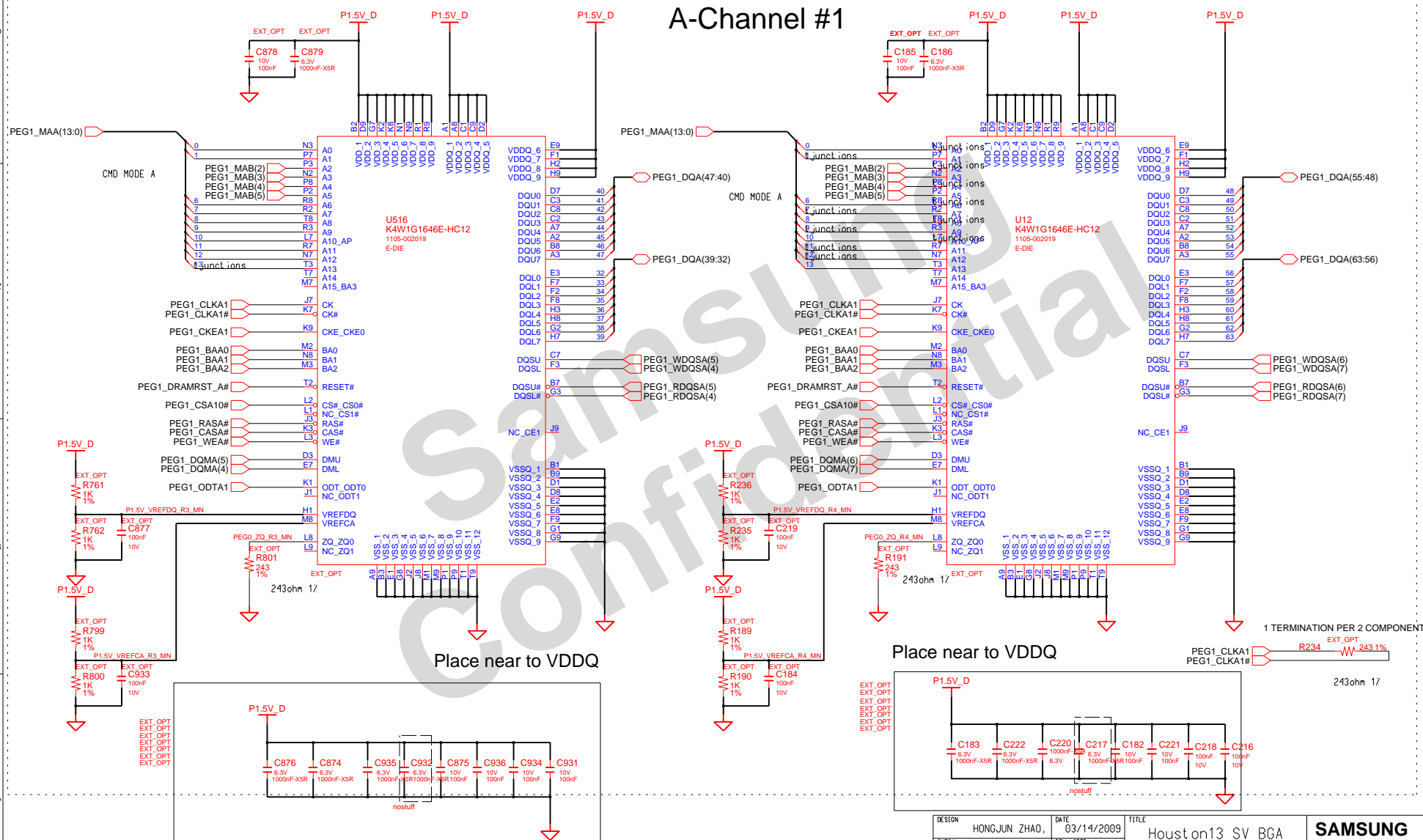


DESIGN	HONGJUN ZHAO,	DATE	03/14/2009	TITLE	Houston13 SV BGA	<b>SAMSUNG</b>	
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		GRAPHIC_MEM A#0	ELECTRONICS	
APPROVAL	BC LEE,	REV	REV 0.0		GRAPHIC_MEM A#0	PART NO.	BA41-#####
MODULE CODE	undefined	LAST EDIT	February, 22, 2010 11:44:42 AM	PAGE	27	OF	53

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## A-Channel #1



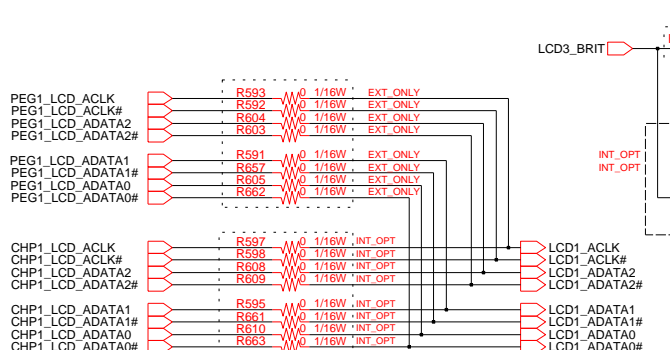
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CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		GRAPHIC_MEM A#1	
APPROVAL	BC LEE,	REV	REV 0.0		GRAPHIC_MEM A#1	
MODULE CODE	undefined	LAST EDIT	February, 22, 2010 11:45:46 AM	PAGE	28 OF 53	

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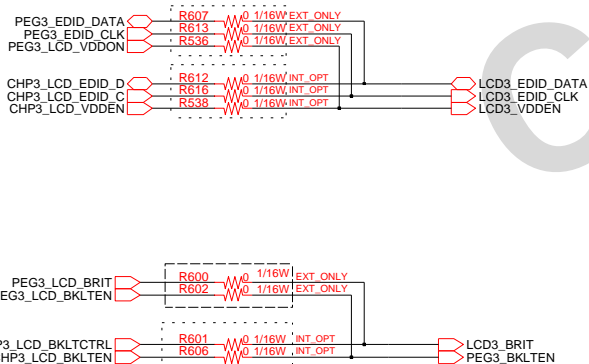
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## LVDS LOGIC 1Ch. LCD Connector + CAMERA

### TSP I/F



### Backlight On



### LCD Power

EBL Purpose

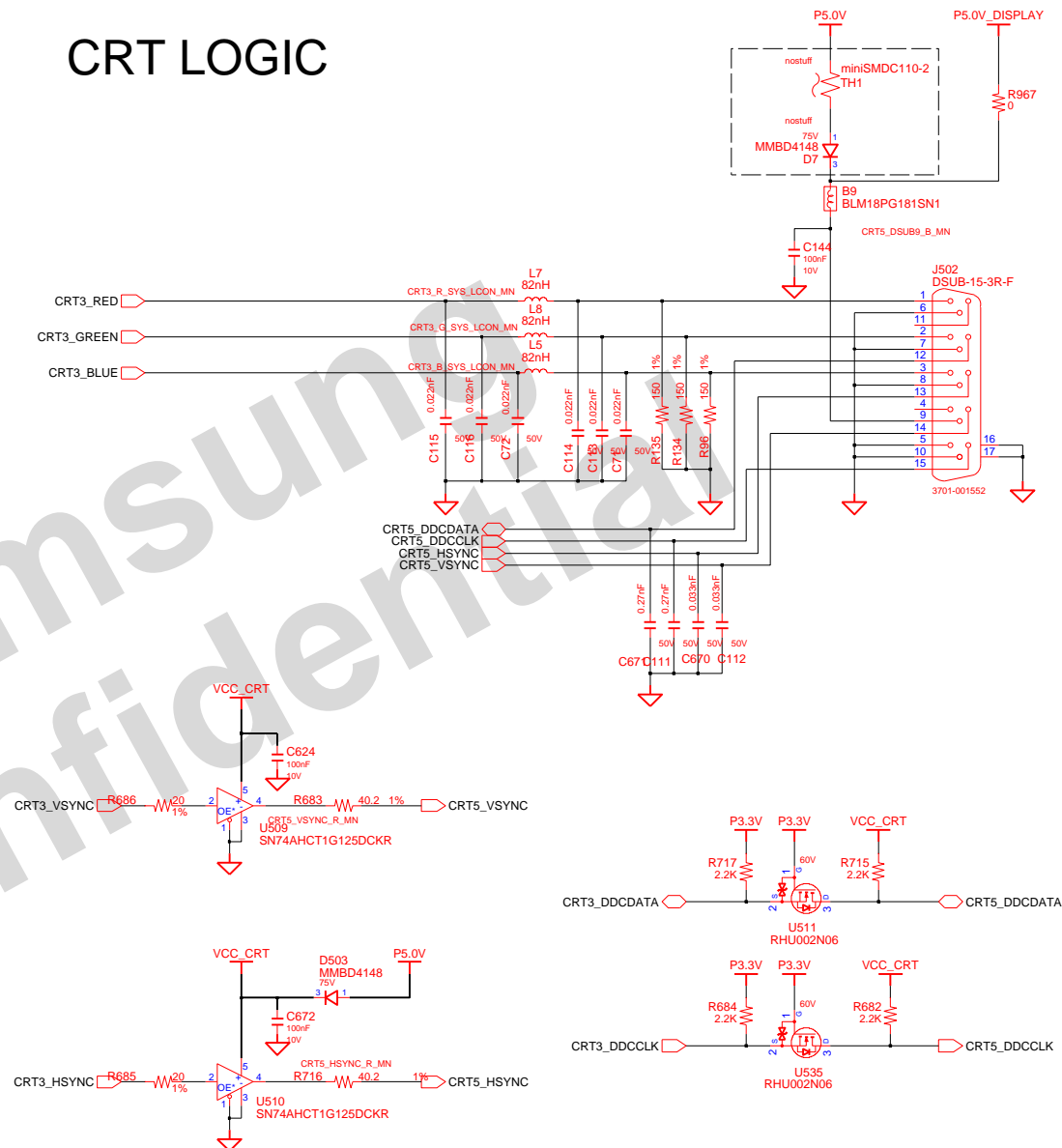
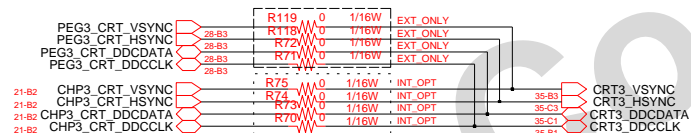
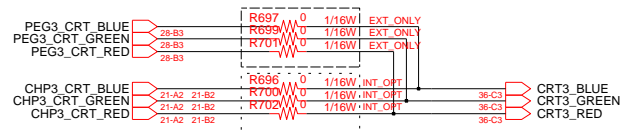
### LED Power

DESIGN	HONGJUN ZHAO,	DATE	9/23/2008	TITLEHouston13 SV BGA		SAMSUNG ELECTRONICS			
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1						
APPROVAL	BC LEE,	REV	REV 0.0	LVDS				PART NO.	BA41-####A
MODULE CODE	undefined		LAST EDIT	February, 22, 2010 11:46:49 AM		PAGE	29	OF	53

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## CRT LOGIC



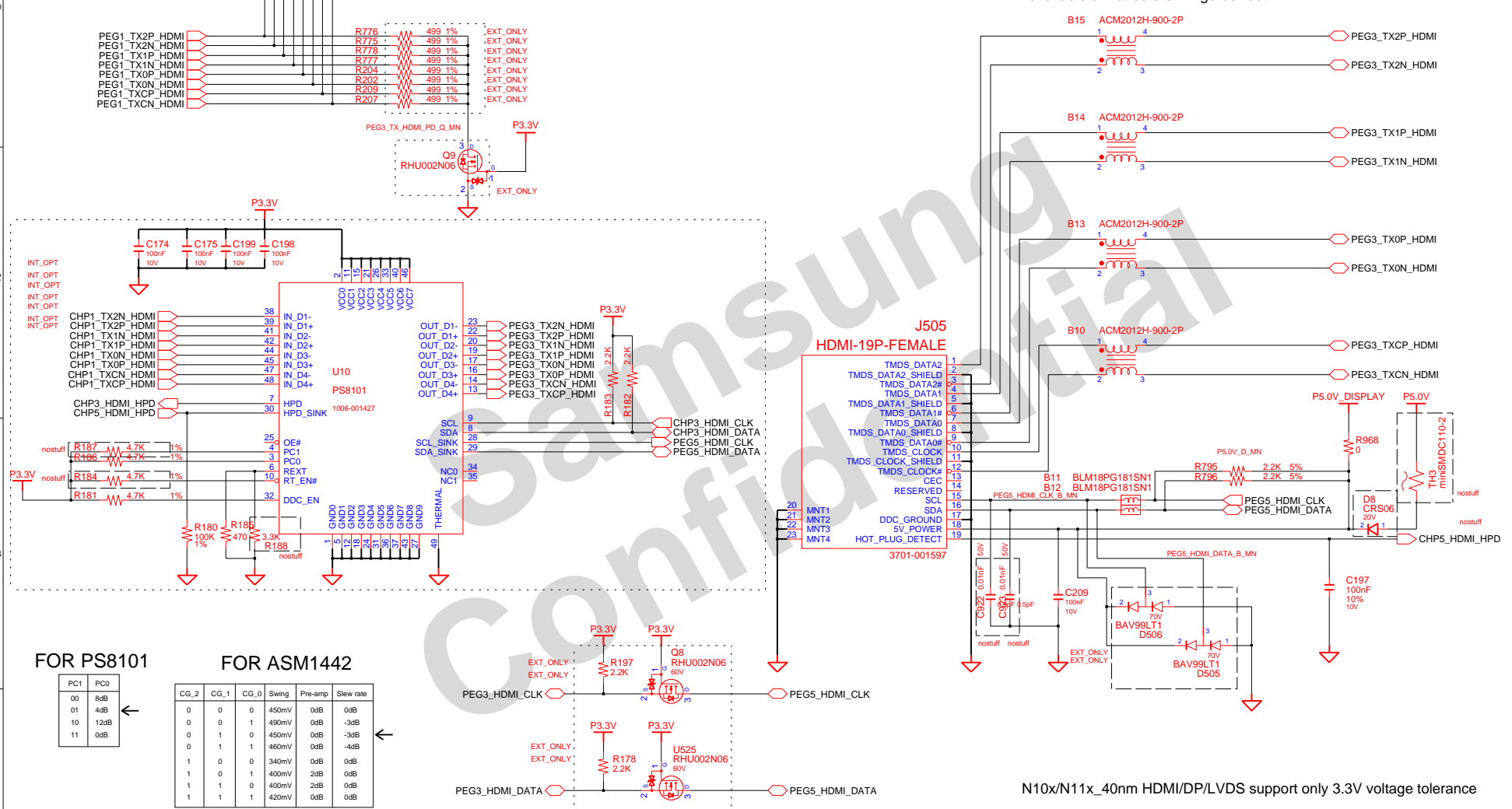
DESIGN	HONGJUN ZHAO,	DATE	9/23/2008	TITLE	Honston13 SV BGA	SAMSUNG ELECTRONICS
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		GRAPHICS_IF	
APPROVAL	BC LEE,	REV	REV 0.0		CRT	
MODULE CODE	undefined	LAST EDIT	February, 22, 2010 11:47:34 AM	PAGE	30	OF 53

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## HDMI Graphic

EMI/SI will confirm which choke is  
available or not before PV gerber-out.



N10x/N11x\_40nm HDMI/DP/LVDS support only 3.3V voltage tolerance

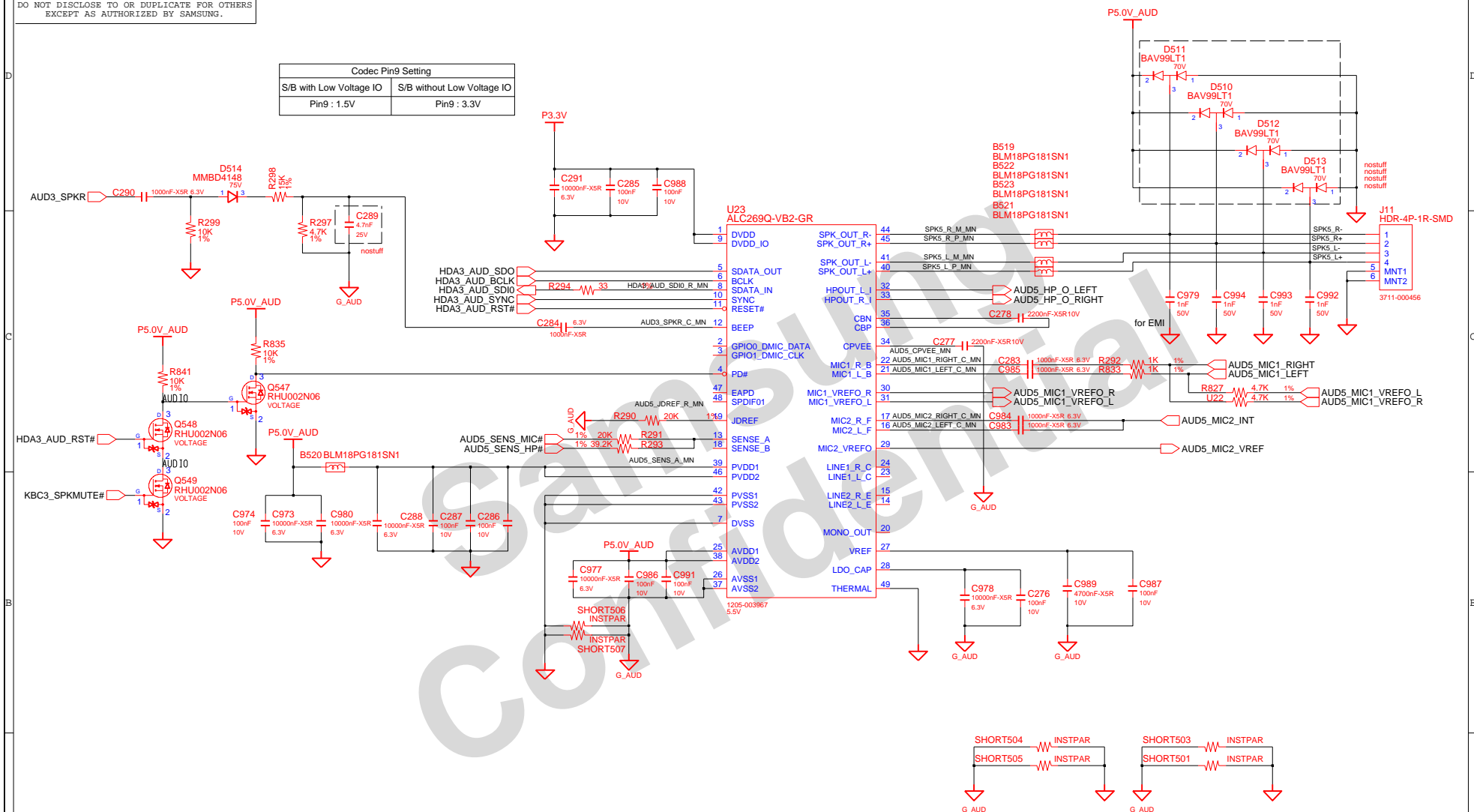
HDMI Level Shifter	REXT(Pin6)	PC1.CG0(Pin3)	PC1.CG1(Pin4)	RT_EN#_CG2(Pin10)	NC_EQ_0(Pin34)	NC_EQ_1(Pin35)	Note	4-6 CODE
PS8101	499 phm	stuff	nostuff	nostuff	NC	NC		1006-001427
ASM1442	3.4K(3.24~3.3K)	nostuff	nostuff	nostuff	nostuff	nostuff	Internal PU/PD exist CGs nostuff is 450mV swing	1006-001471

DESIGN	HONGJUN ZHAO,	DATE	9/23/2008	TITLE	Honston13 SV BGA	SAMSUNG
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		GRAPHICS_IF	ELECTRONICS
APPROVAL	BC LEE,	REV	REV 0.0		HDMI	PART NO.
MODULE CODE	undefined	LAST EDIT	February, 22, 2010 11:48:26 AM			BA41-####A
			PAGE	31	OF	53



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Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V



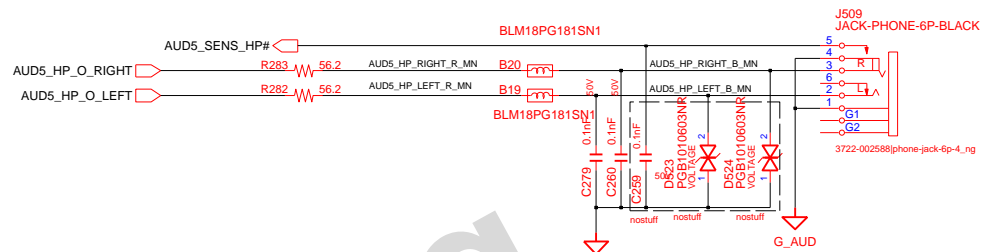
DESIGN	HONGJUN ZHAO,	DATE	9/23/2008	TITLE Houston13 SV BGA HDA_CODEC AUDIO CODEC ALC269	<b>SAMSUNG</b> ELECTRONICS
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		
APPROVAL	BC LEE,	REV	REV 0.0		
MODULE CODE	undefined	LAST EDIT	February, 22, 2010 11:49:10 AM		
				PAGE	32 OF 53



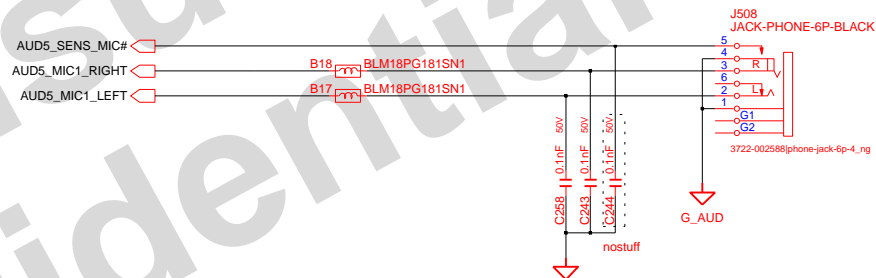
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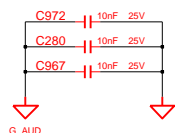
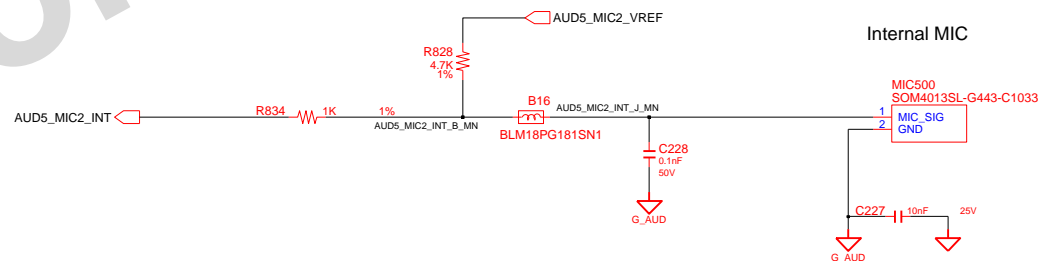
## HEADPHONE



## MIC JACK



## Internal MIC



DESIGN	HONGJUN ZHAO,	DATE	9/23/2008	TITLE	Houston13 SV BGA	SAMSUNG ELECTRONICS
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		HDA_CODEC	
APPROVAL	BC LEE,	REV	REV 0.0		AUDIO JACK	
MODULE CODE	undefined	LAST EDIT	February, 22, 2010 11:50:03 AM	PAGE	33	OF 53

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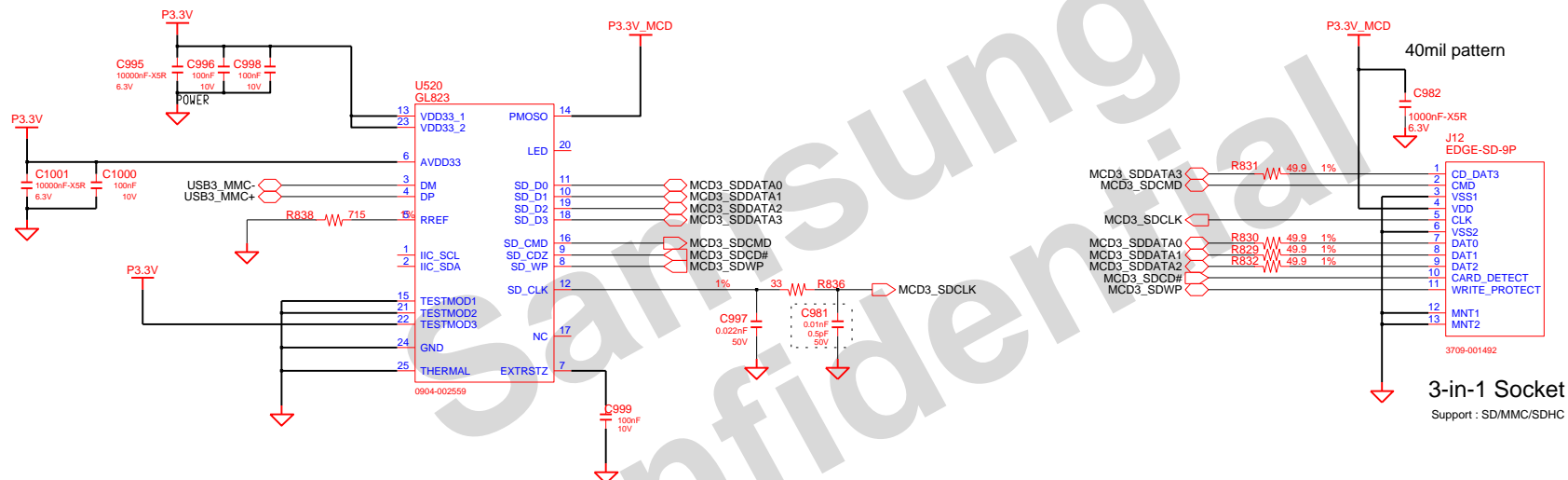
[illegible]

DESIGN	HONGJUN ZHAO,	DATE	9/23/2008	TITLE	Houston13 SV BGA	<b>SAMSUNG</b>	
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		LAN	ELECTRONICS	
APPROVAL	BC LEE,	REV	REV 0.0		LAN_Realtek_RTL8103EL	PART NO.	BA41-####A
MODULE CODE	undefined	LAST EDIT	February, 22, 2010 11:51:14 AM		PAGE	34	OF 53

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## 2 IN 1 CARD (GL823)

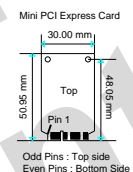
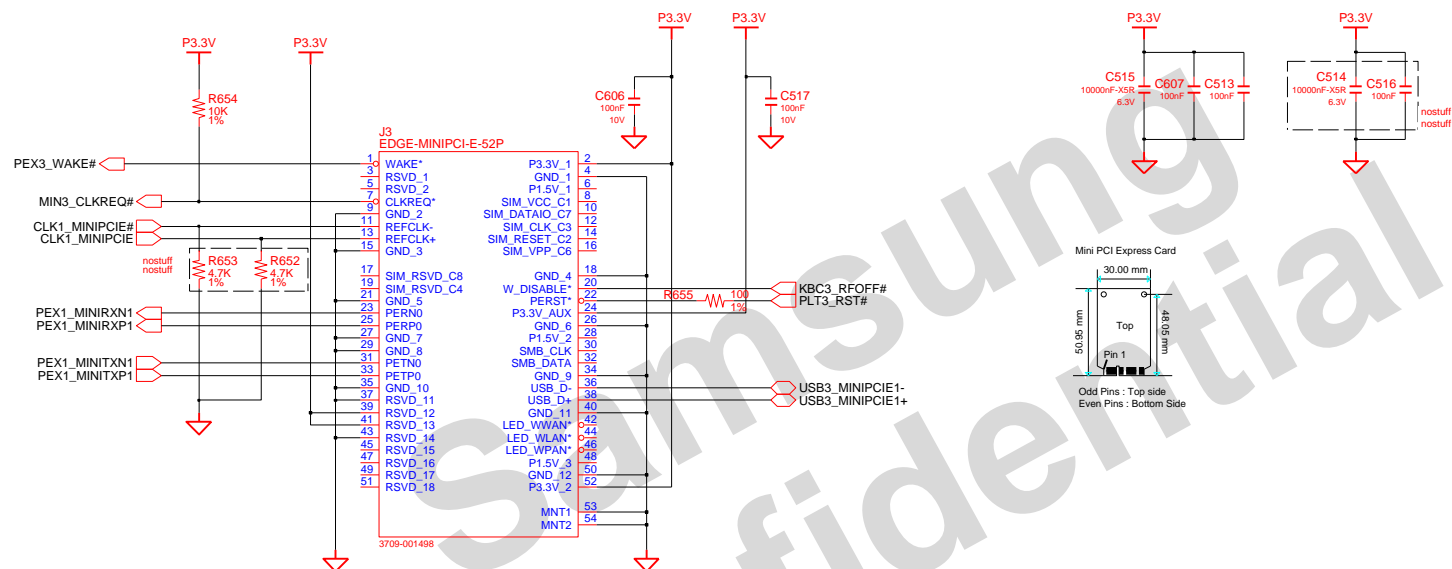


Cost down 0.014\$ to AU6366

DESIGN	HONGJUN ZHAO,	DATE	9/23/2008	Houston13 SV BGA MULTICARD 3 IN 1 CARD(GL827S)		SAMSUNG ELECTRONICS			
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1						
APPROVAL	BC LEE,	REV	REV 0.0						
MODULE CODE		LAST EDIT		February, 22, 2010 11:53:09 AM		PAGE	35	OF	53
undefined									

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AMT 6.0 : P3.3V = P3.3V\_ALW (Check?)  
wakeup pull-up power rail ?  
Puma Peak -WiFi (AMT 6.0)  
Kilmer Peak - WiFi/WiMax

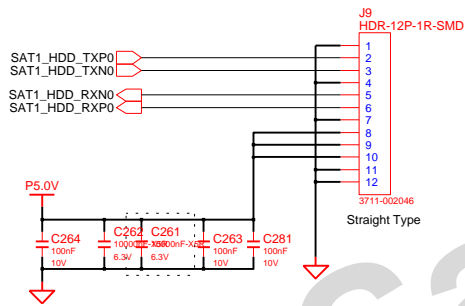


DESIGN	HONGJUN ZHAO,	DATE	9/23/2008	TITLE		Houston13 SV BGA		<b>SAMSUNG</b> ELECTRONICS	
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1						
APPROVAL	BC LEE,	REV	REV 0.0	MINI_PCIE_CONN WLAN		PART NO.		BA41-####A	
MODULE CODE	undefined	LAST EDIT				February, 22, 2010 11:53:59 AM		PAGE	36

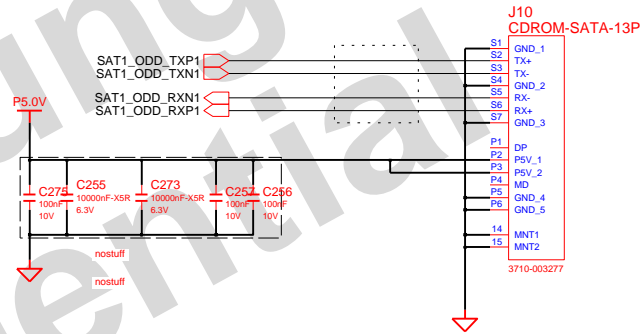
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# SATA I/F CONN

SATA HDD CONN



MAIN TO SUB SATA ODD CONN



DESIGN	HONGJUN ZHAO,	DATE	9/23/2008	TITLE	Houston13 SV BGA	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-####A
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		SATA_DEVICES	
APPROVAL	BC LEE,	REV	REV 0.0		HDD & ODD SUB CONNECTOR	
MODULE CODE	undefined	LAST EDIT	February, 22, 2010 11:58:42 AM	PAGE	37 OF 53	

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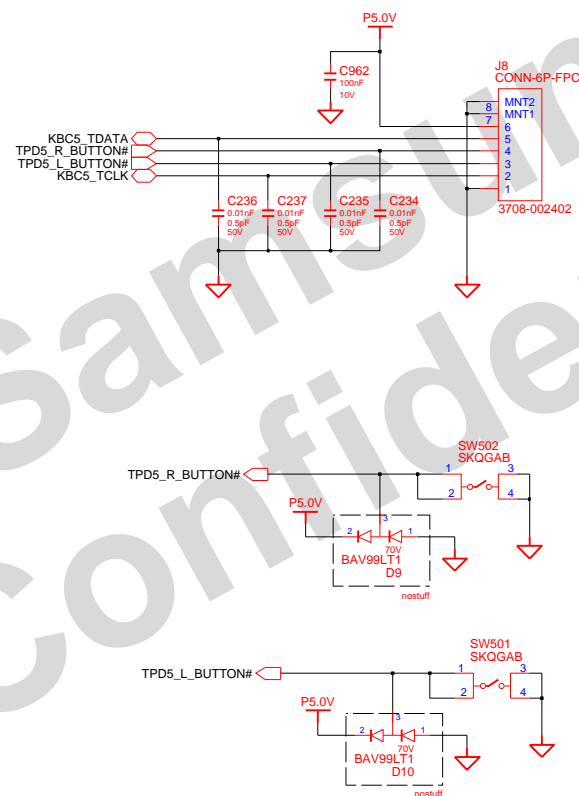
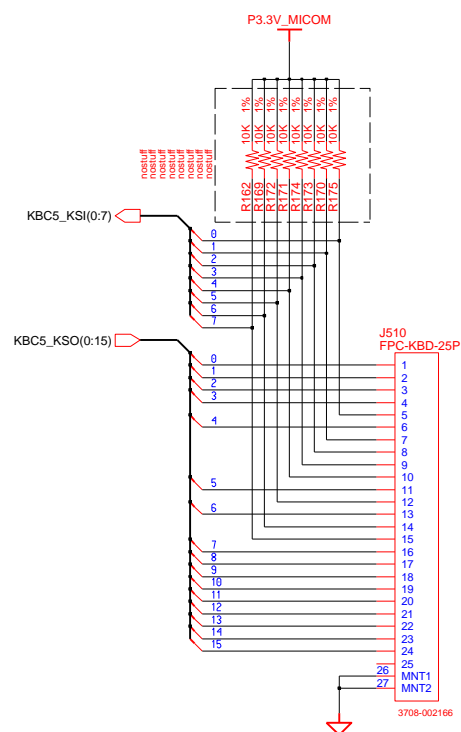



DRAM	HONGJUN ZHAO,	DATE	11/17/2008	Houston13 SV BGA M1COM MICOM_SMSC_MEC1308		<b>SAMSUNG</b> ELECTRONICS	
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1				
APPROVAL	BC LEE,	REV	REV 0.0			PART NO.	BA14-#####
MODULE CODE	LAST EDIT		February, 22, 2010 11:59:12 AM			PAGE	38 OF 53

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# Micom Glue Logic

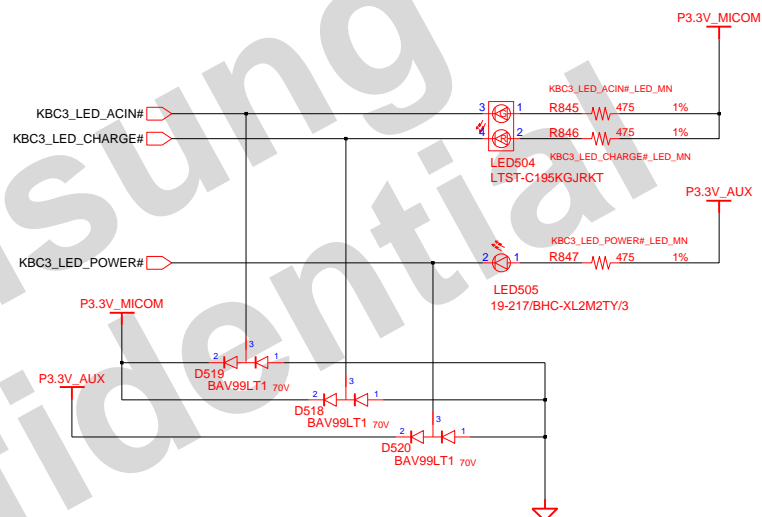
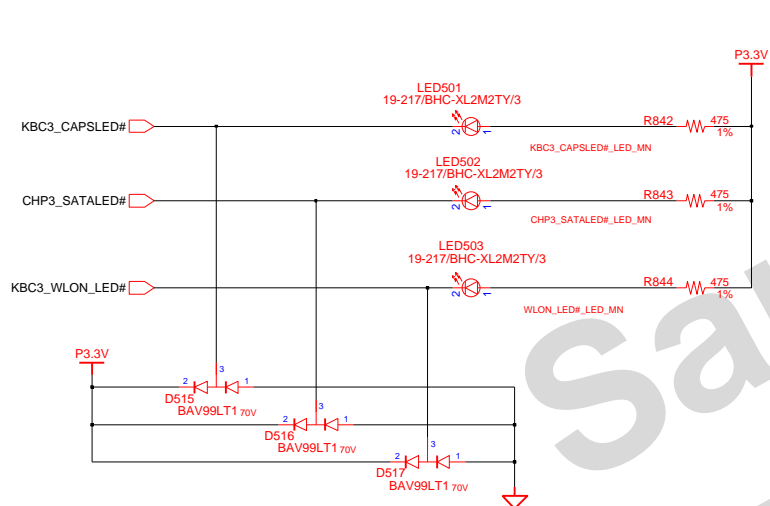
## TOUCHPAD



DESIGN	HONGJUN ZHAO,	DATE	9/23/2008	TITLE	Houston13 SV BGA		
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		MICOM GLUE LOGIC		
APPROVAL	BC LEE,	REV	REV 0.0	KETBOARD & TOUCHPAD		PART NO.	BA41-####A
MODULE CODE	undefined	LAST EDIT	February, 22, 2010 12:02:24 PM			PAGE	39 OF 53

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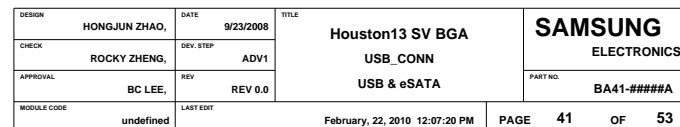
**FUNCTION KEY LED****ADAPTERIN/CHARGING LED**

DRAW	HONGJUN ZHAO,	DATE	9/23/2008	TITLE	Houston13 SV BGA	SAMSUNG ELECTRONICS	
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1				LED_SWITCH
APPROVAL	BC LEE,	REV	REV 0.0				LED_SWITCH
				PART NO.	BA41-####A		
MODULE CODE	LAST EDIT			February, 22, 2010 12:03:11 PM	PAGE 40 OF 53		



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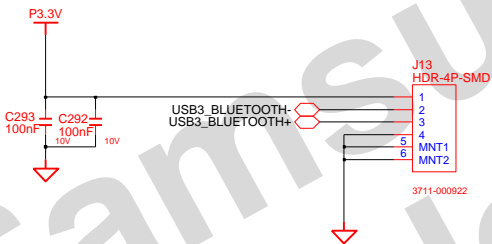
## USB SUB B'D CONNECTOR



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# USB I/F Devices

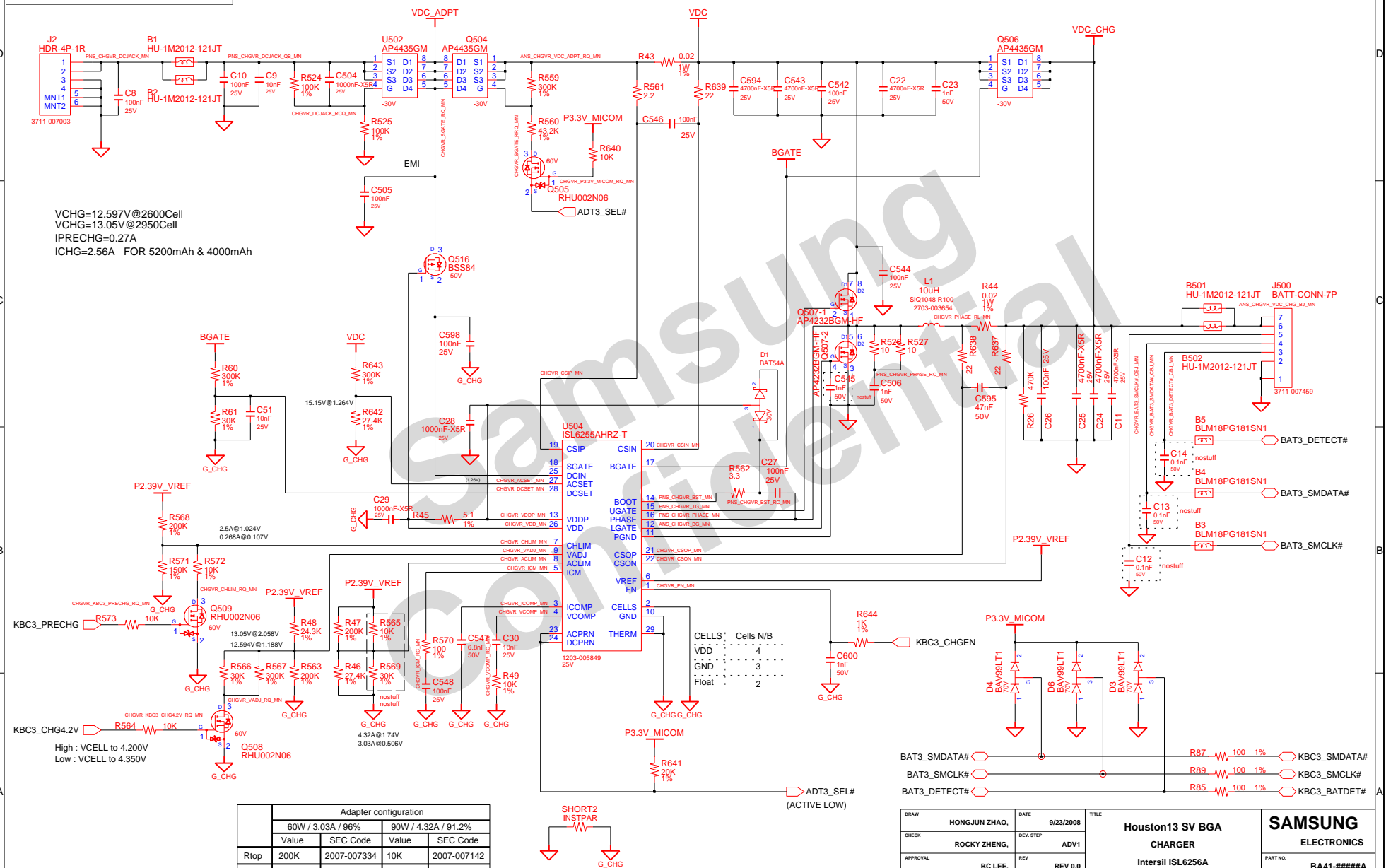
## Bluetooth Interface



DESIGN	HONGJUN ZHAO,	DATE	9/23/2008	TITLE	Houston13 SV BGA	<b>SAMSUNG</b> ELECTRONICS
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		USB_DEVICES	
APPROVAL	BC LEE,	REV	REV 0.0		BLUETOOTH & CAMERA	
MODULE CODE	undefined	LAST EDIT	February, 22, 2010 12:08:32 PM			
					PAGE 42 OF 53	PART NO. BA41-####A

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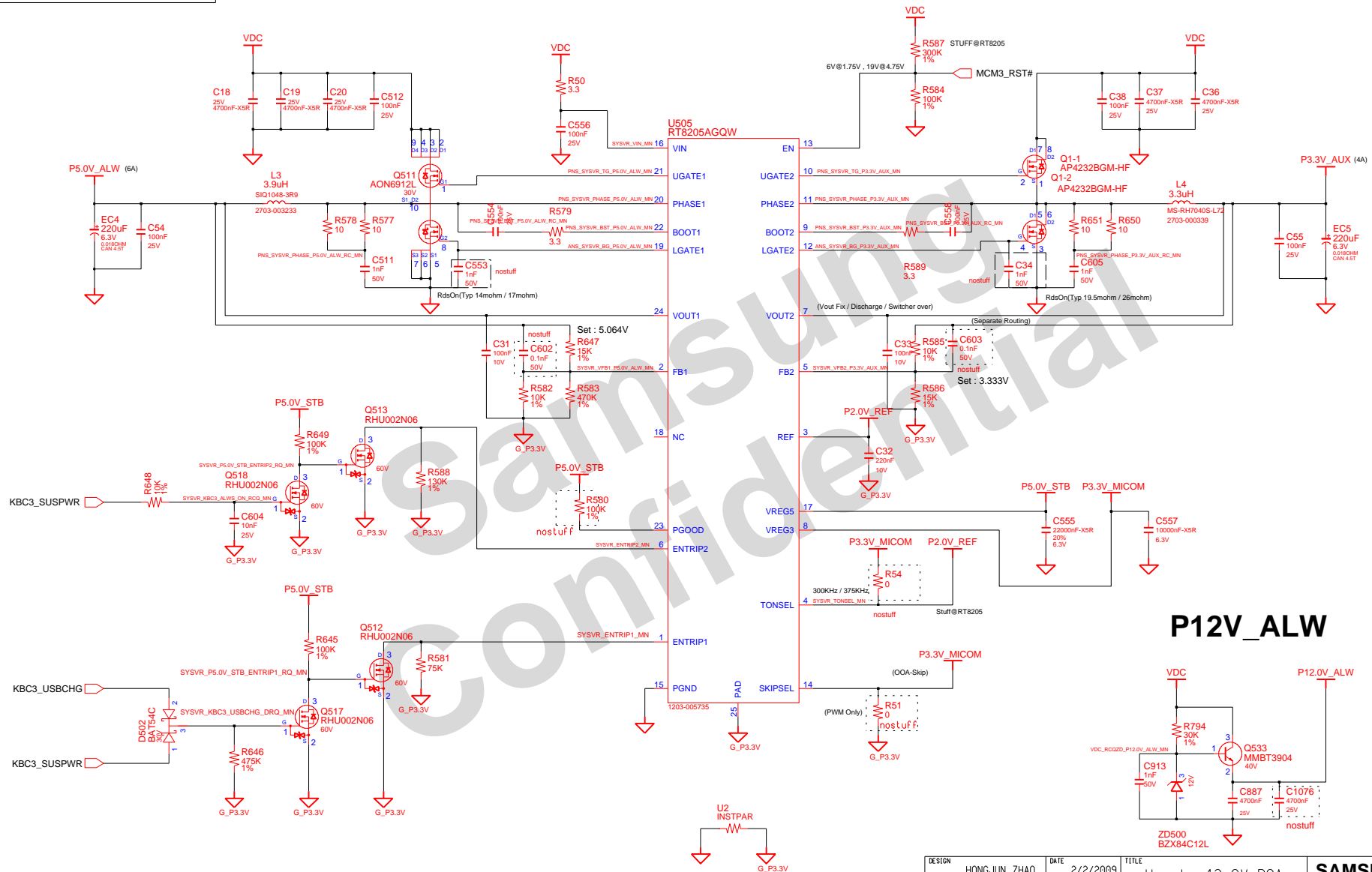
# CHARGER & POWER MANAGEMENT



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## P3.3V\_AUX & P5.0V\_ALW



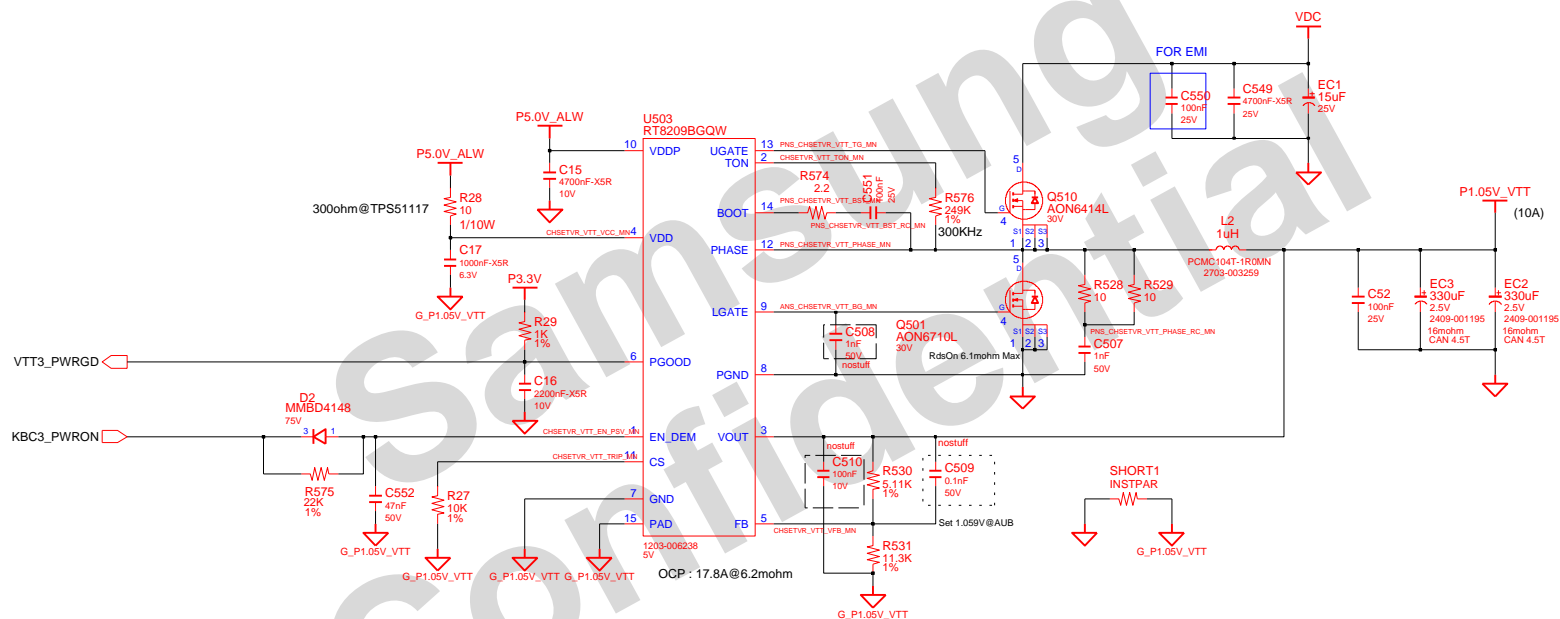
**P5.0V\_AUX Inductor: 10x10x4.8**  
**P3.3V\_AUX Inductor: 7x7x4 (5.2A)**  
**Output Cap: 6x6x4.5**

DESIGN	HONGJUN ZHAO,	DATE	2/2/2009	TITLE	Houston13 SV BGA	SAMSUNG ELECTRONICS
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		P3.3V_AUX / P5.0V_ALW	
APPROVAL	BC LEE,	REV	REV 0.0		TI TPS51125	
MODULE CODE	undefined	LAST EDIT	February, 22, 2010 12:11:35 PM	PAGE	44 OF 53	

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## Chipset Power (P1.05V)



DRAW	HONGJUN ZHAO,	DATE	01/09/2008	TITLE	Houston13 SV BGA	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-####A
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		P1.05V	
APPROVAL	BC LEE,	REV	REV 0.0		TI TPS51125	
MODULE CODE	undefined	LAST EDIT	February, 22, 2010 12:12:12 PM	PAGE	45 OF 53	

## DDR3 Power

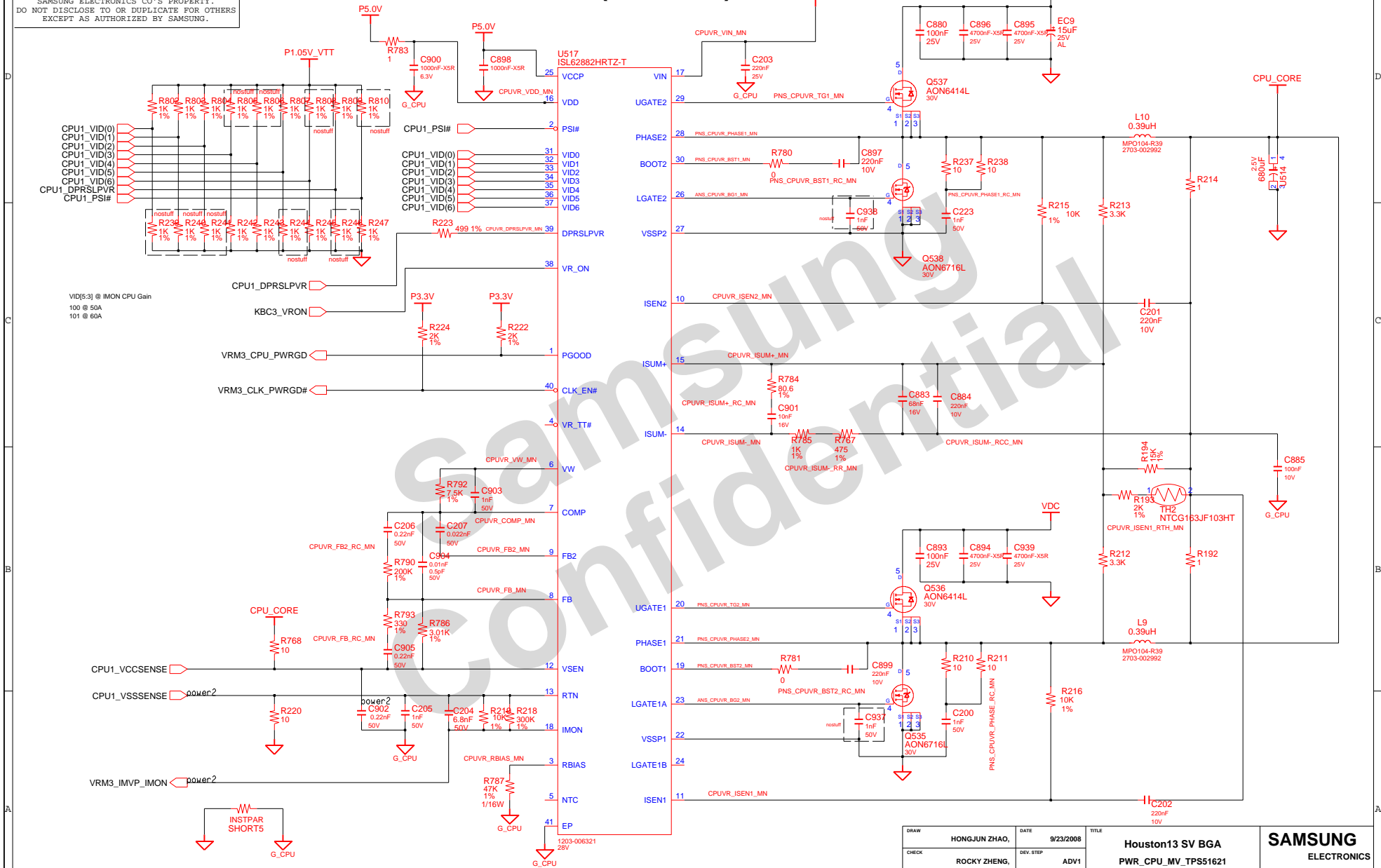
[illegible]

COM-22C-015(1996.6.5) REV. 3

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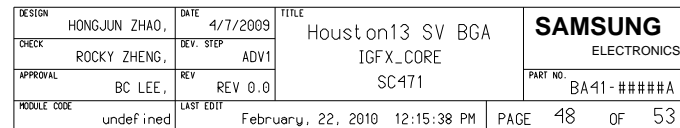
## CPU VRM (IMVP-6.5)



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```
IMON GPU Gain Setting
VID0 (1) : Reserved
VID1 (1) : Reserved
VID2 (1) : Reserved
VID3 (1) : IMON
VID4 (0) : IMON , 20A
VID5 (0) : IMON
VID6 (0) : Reserved
DPRSLPVR(1) : IMVP6.5
```

BootVoltage Set : 0.90V



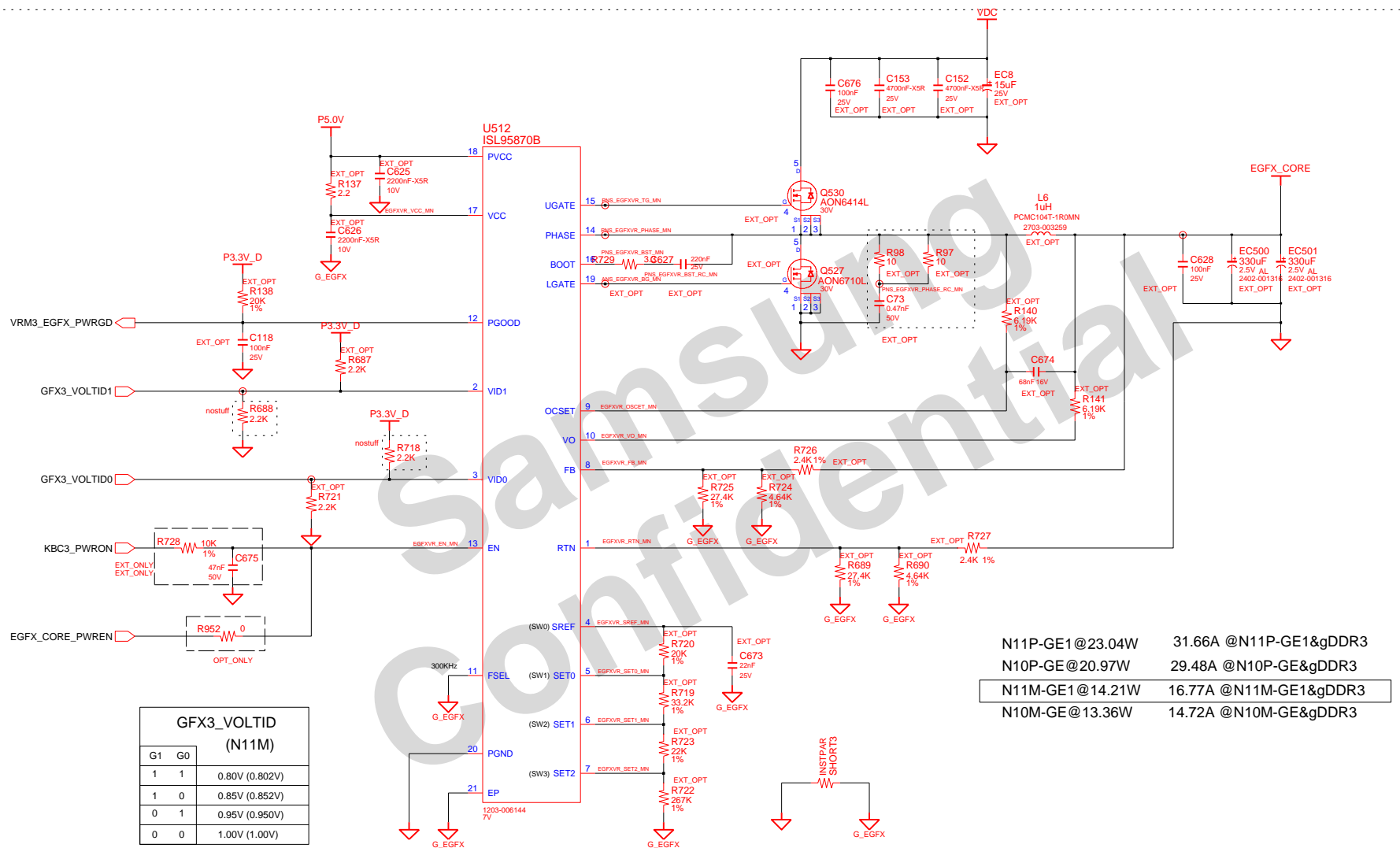


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EXT\_OPT

## External GFX Core Power



N11P-GE1@23.04W 31.66A @N11P-GE1&gDDR3  
N10P-GE@20.97W 29.48A @N10P-GE&gDDR3  
N11M-GE1@14.21W 16.77A @N11M-GE1&gDDR3  
N10M-GE@13.36W 14.72A @N10M-GE&gDDR3

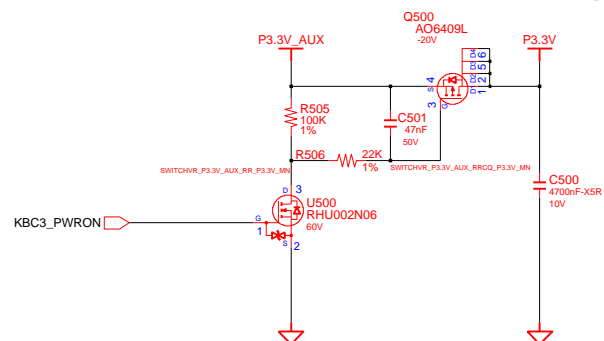
DRAW	HONGJUN ZHAO,	DATE	9/23/2008	TITLE	Houston13 SV BGA	SAMSUNG ELECTRONICS
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		EGFX_CORE	
APPROVAL	BC LEE,	REV	REV 0.0			PART NO. BA41-####A
MODULE CODE	undefined	LAST EDIT	February, 22, 2010 12:16:30 PM	PAGE	49	OF 53

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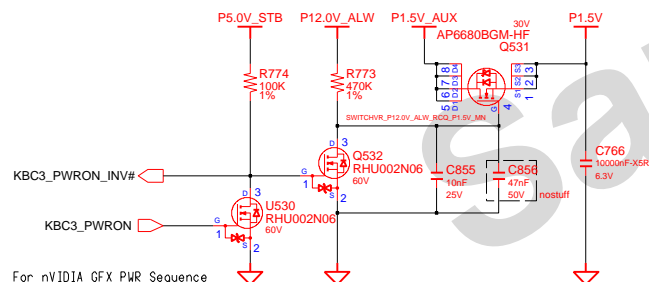
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# Switched Power 1

## Switched Power On (P3.3V) Multi@AP2607GY,Si3433BDV



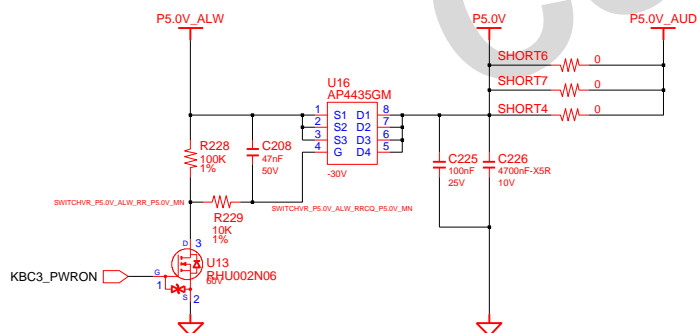
## Switched Power On (P1.5V)



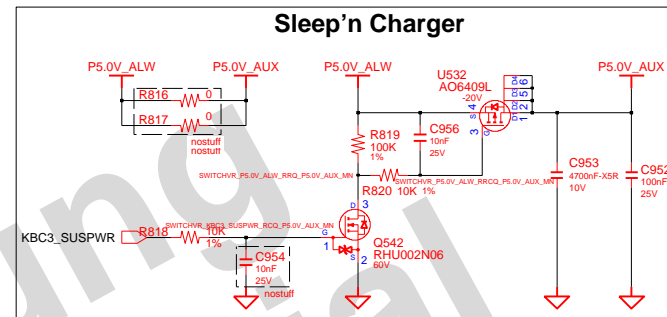
For nVIDIA GFX PWR Sequence

NVDD(EGFX\_CORE) first and then FBVDDQ(gDDR3)

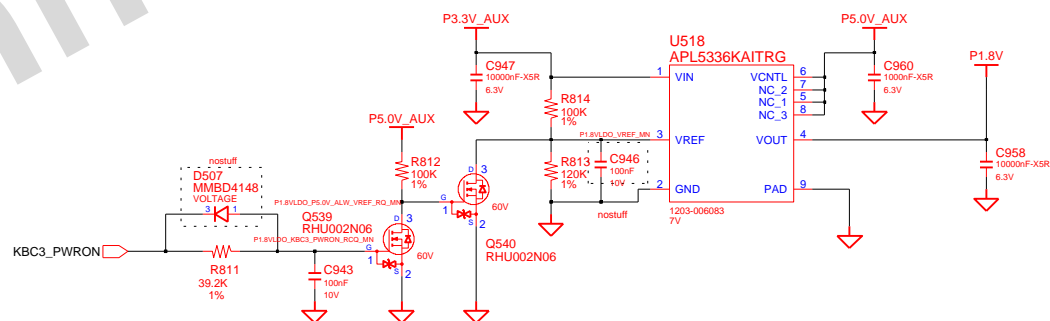
## Switched Power On (P5.0V) Multi@Si443DDY



## Sleep'n Charger



## P1.8V(LDO)



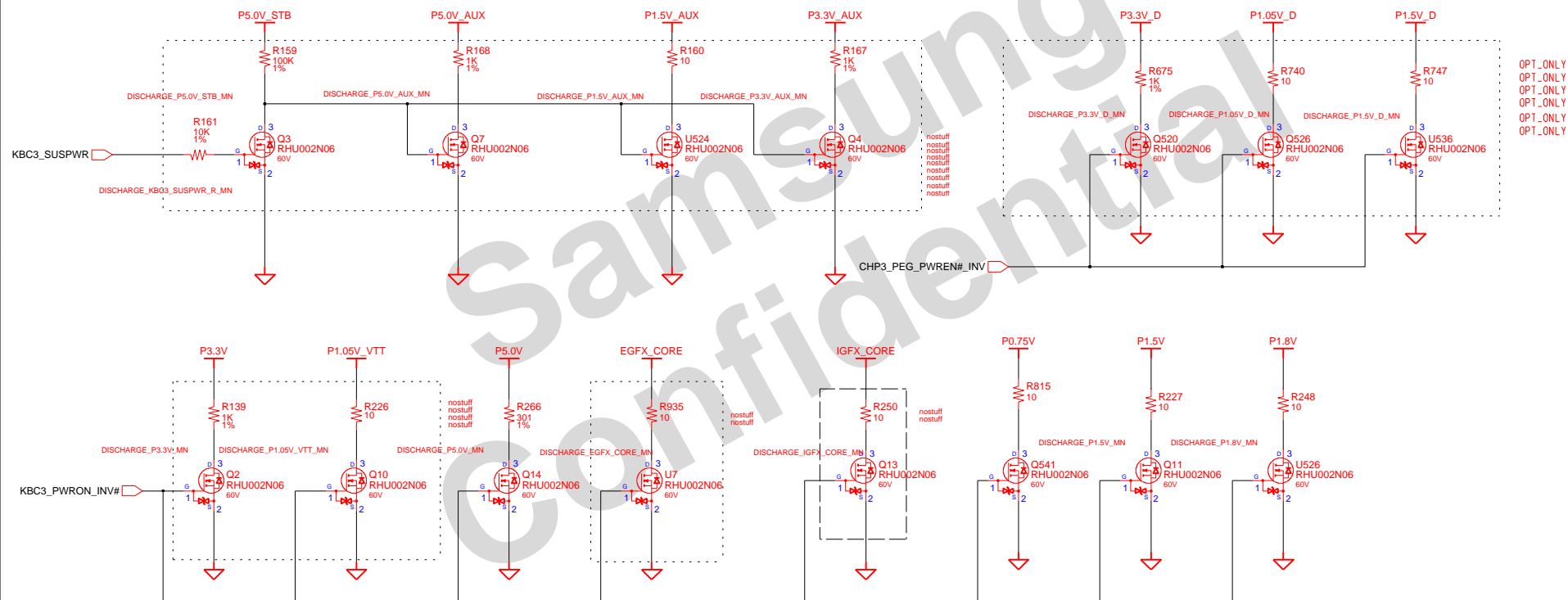
DRAW	HONGJUN ZHAO,	DATE	9/23/2008	TITLE	Houston13 SV BGA
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		PWR_MV_SWITCHED
APPROVAL	BC LEE,	REV	REV 0.0		SWITCHED POWER
MODULE CODE	undefined	LAST EDIT	February, 22, 2010 12:34:53 PM	PAGE	50 OF 53

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BA41-####A

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## Power DisCharge

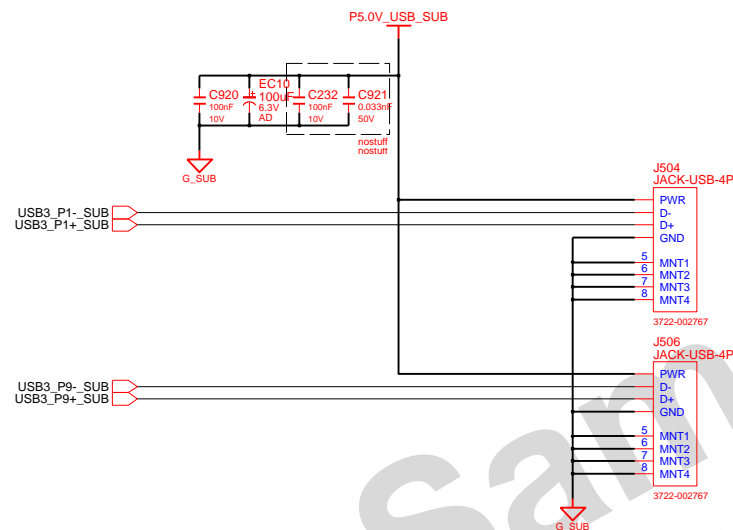


DRAW	HONGJUN ZHAO,	DATE	10/30/2008	TITLE	Houston13 SV BGA	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-####A
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		LPC_TPM_1p2	
APPROVAL	BC LEE,	REV	REV 0.0		LPC_TPM_1p2	
MODULE CODE	undefined	LAST EDIT	February, 22, 2010 12:35:29 PM	PAGE	51	OF 53

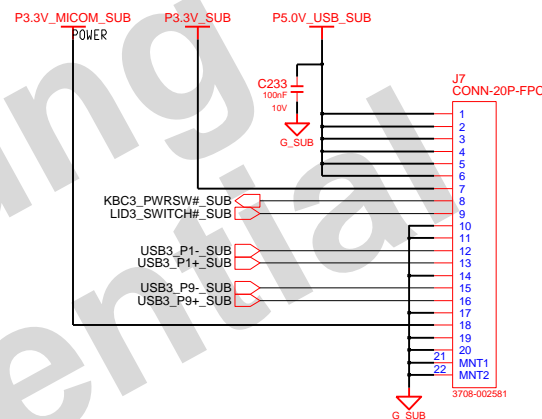
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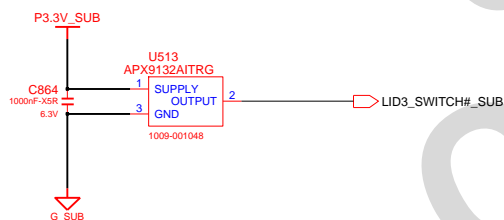
## 2 USB PORT & POWER S/W SUB B'D



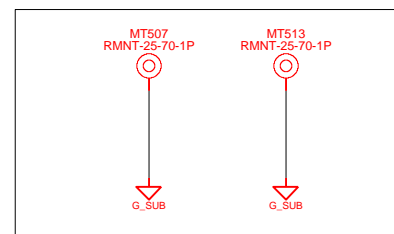
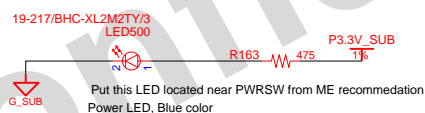
### SUB TO MAIN USB CONN



### LID\_SWITCH

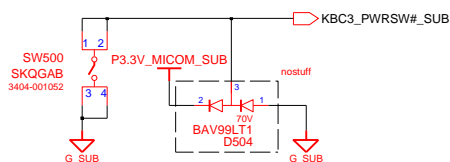


### Power ON LED



USB sub board mount hole

### Power Switch Button



DESIGN	HONGJU ZHAO,	DATE	9/23/2008	TITLE	Houston13 SV BGA SUB BOARD1 2 USB & POWER SW	SAMSUNG ELECTRONICS
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1			PART NO. BA41-####A
APPROVAL	BC LEE,	REV	REV 0.0			
MODULE CODE	undefined	LAST EDIT	February, 22, 2010 12:36:28 PM	PAGE	52	OF 53

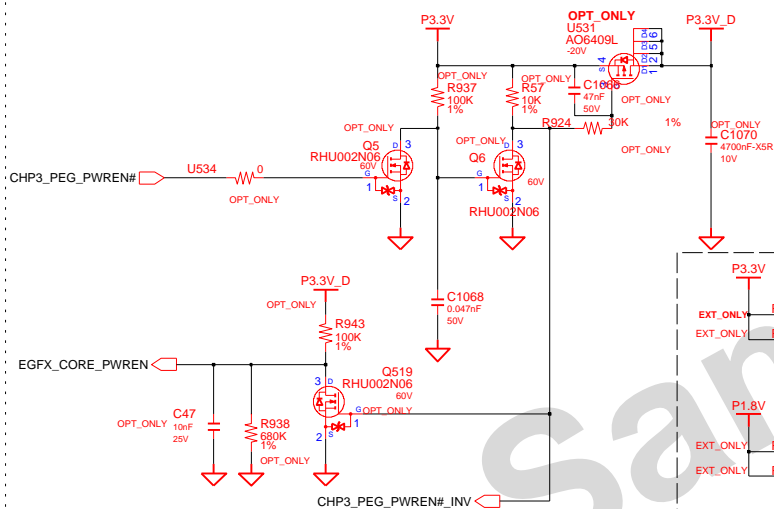
# Switched Power 2 (For nVidia GFX Power Sequence)

Sequence (D3.3V -> GFX Core -> D1.8V -> D1.5V -> D1.05V)

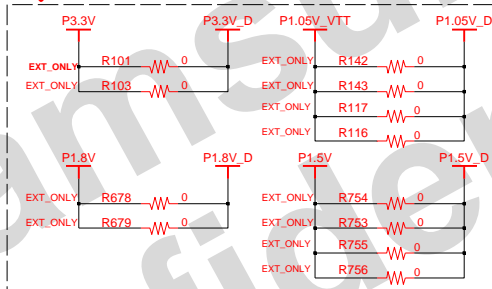
OPT\_ONLY

Discrete Switched Power (D3.3V : Max\_1.2A)

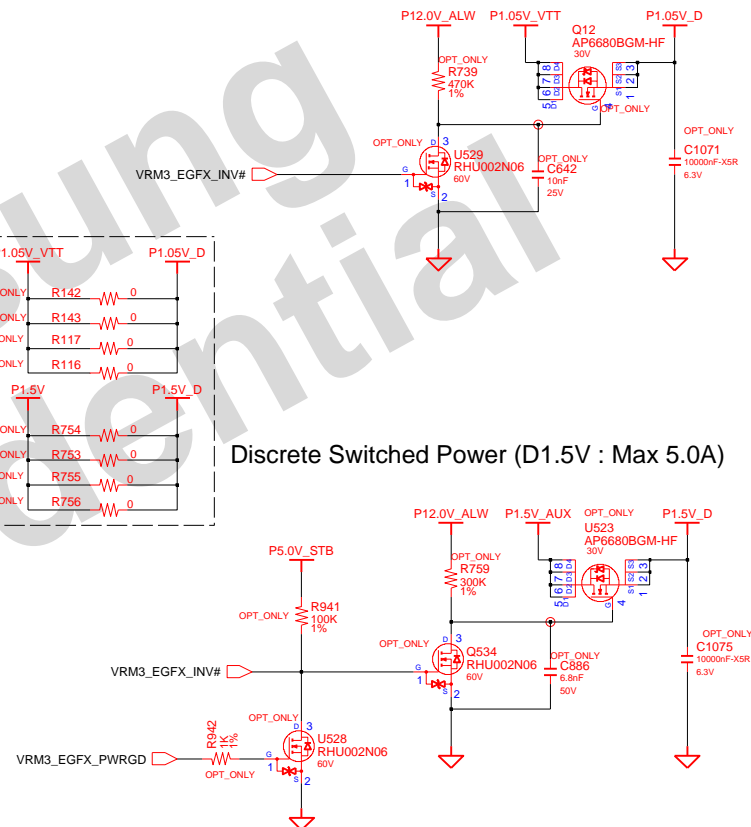
Discrete Switched Power (D1.05V : Max 3.6A)



EXT\_ONLY

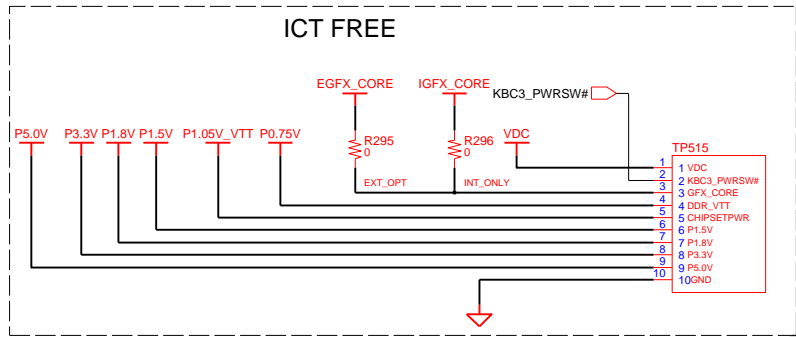


Discrete Switched Power (D1.5V : Max 5.0A)

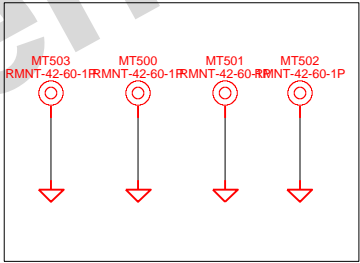
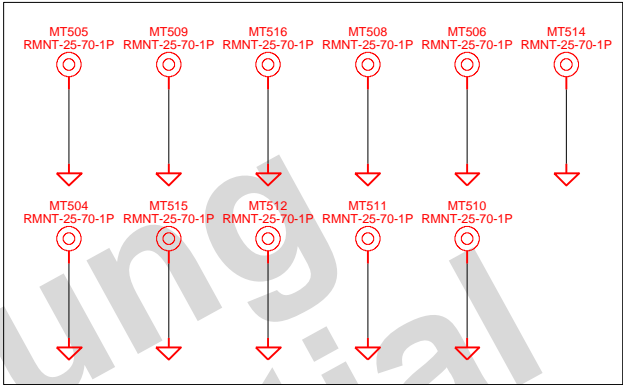


DRW	HONGJUN ZHAO,	DATE	10/30/2008	TITLE	Houston13 SV BGA	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-####A
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		LPC_TPM_1p2	
APPROVAL	BC LEE,	REV	REV 0.0		LPC_TPM_1p2	
MODULE CODE	undefined	LAST EDIT	February, 22, 2010 12:35:29 PM	PAGE	51 OF 53	

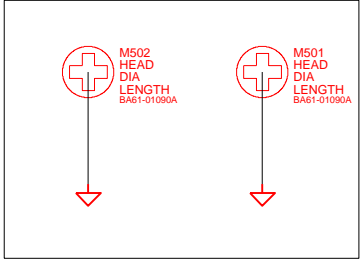
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Mainboard Mount ((25,70)x12EA)



CPU Thermal



GPU Thermal

DRAW	HONGJUN ZHAO,	DATE	9/23/2008	TITLE	Houston13 SV BGA	SAMSUNG ELECTRONICS
CHECK	ROCKY ZHENG,	DEV. STEP	ADV1		ICT PORT	
APPROVAL	BC LEE,	REV	REV 0.0		ICT PORT	
MODULE CODE		LAST EDIT		February, 22, 2010 12:37:07 PM	PAGE 53 OF 53	PART NO. BA41-####A